

After writing the first page and before writing the second page

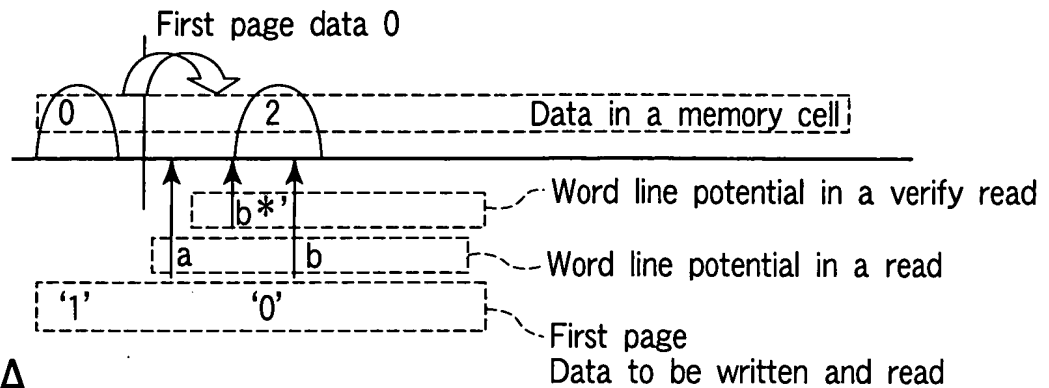


FIG. 1A

Before writing the second page and after writing the adjacent cells

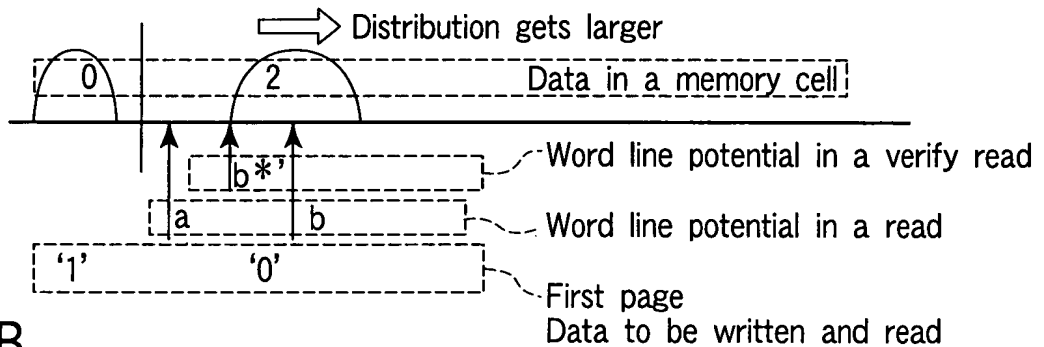


FIG. 1B

After writing the second page

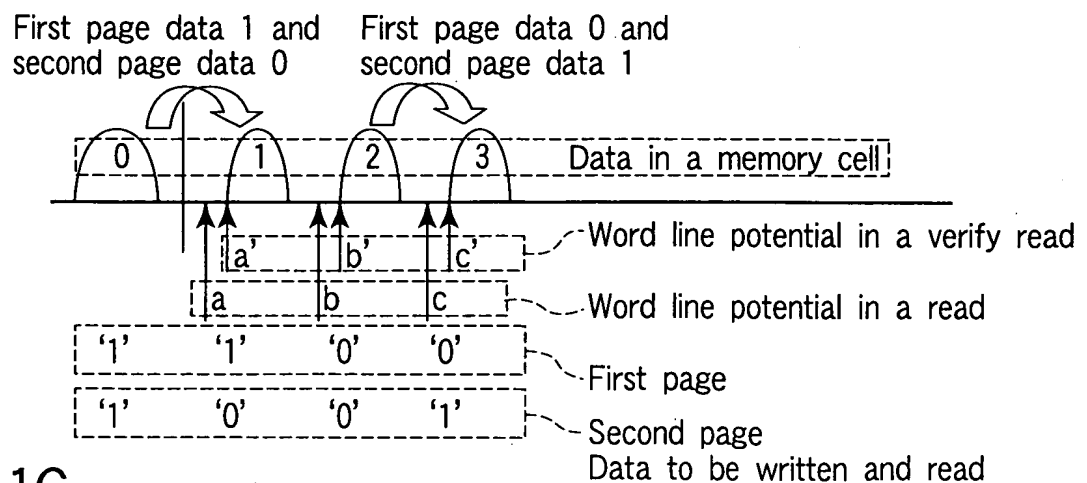


FIG. 1C

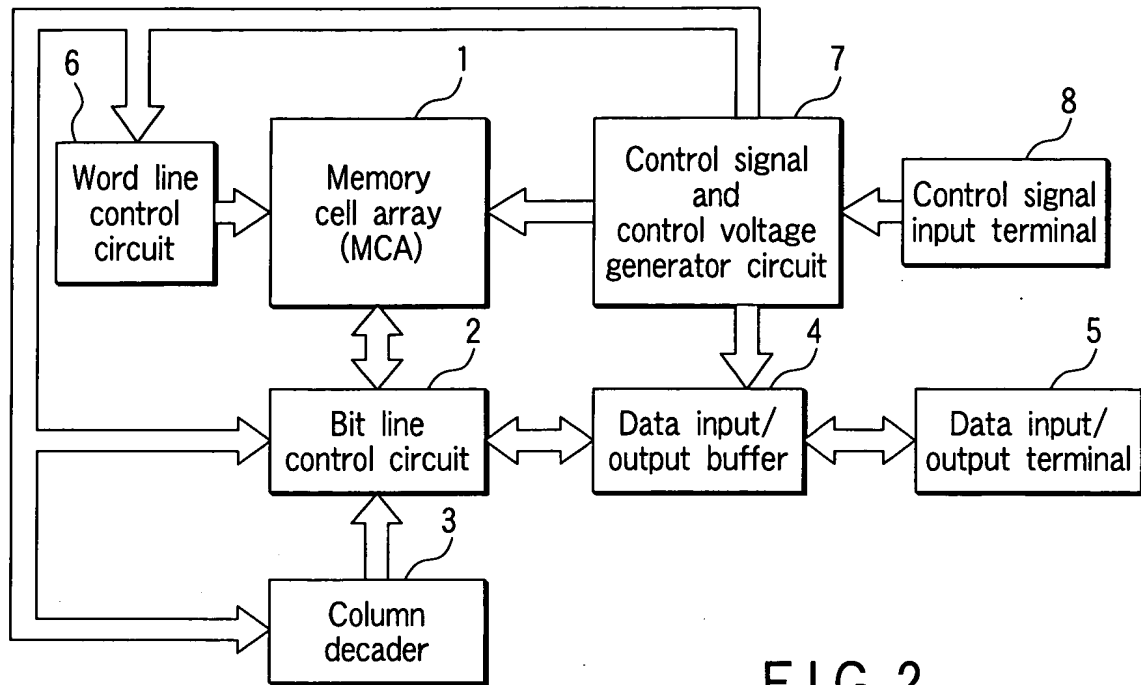


FIG. 2

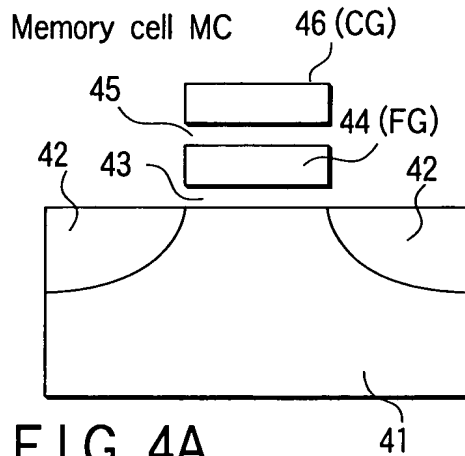


FIG. 4A

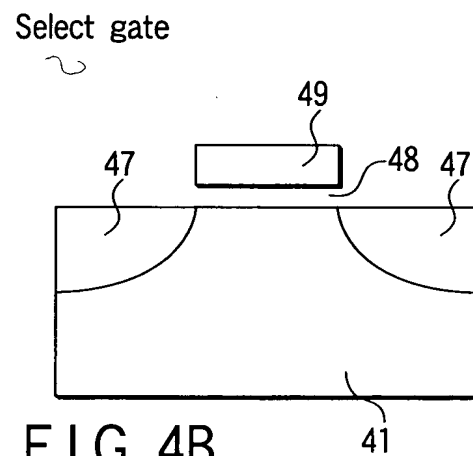


FIG. 4B

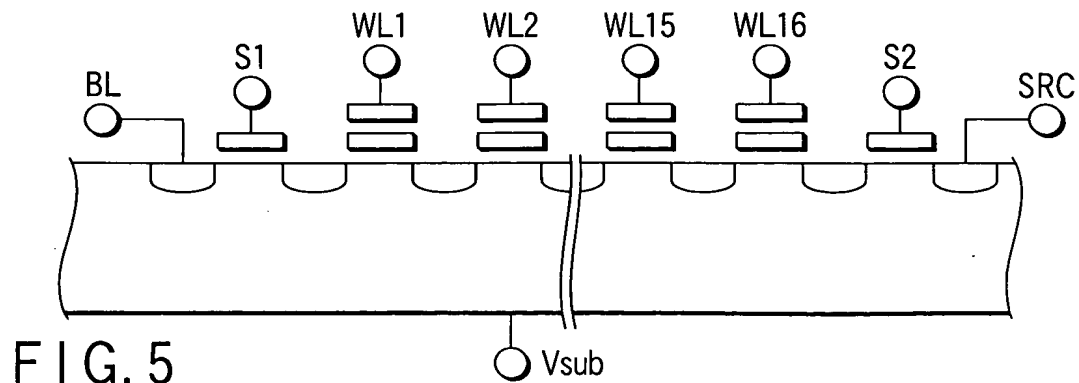


FIG. 5

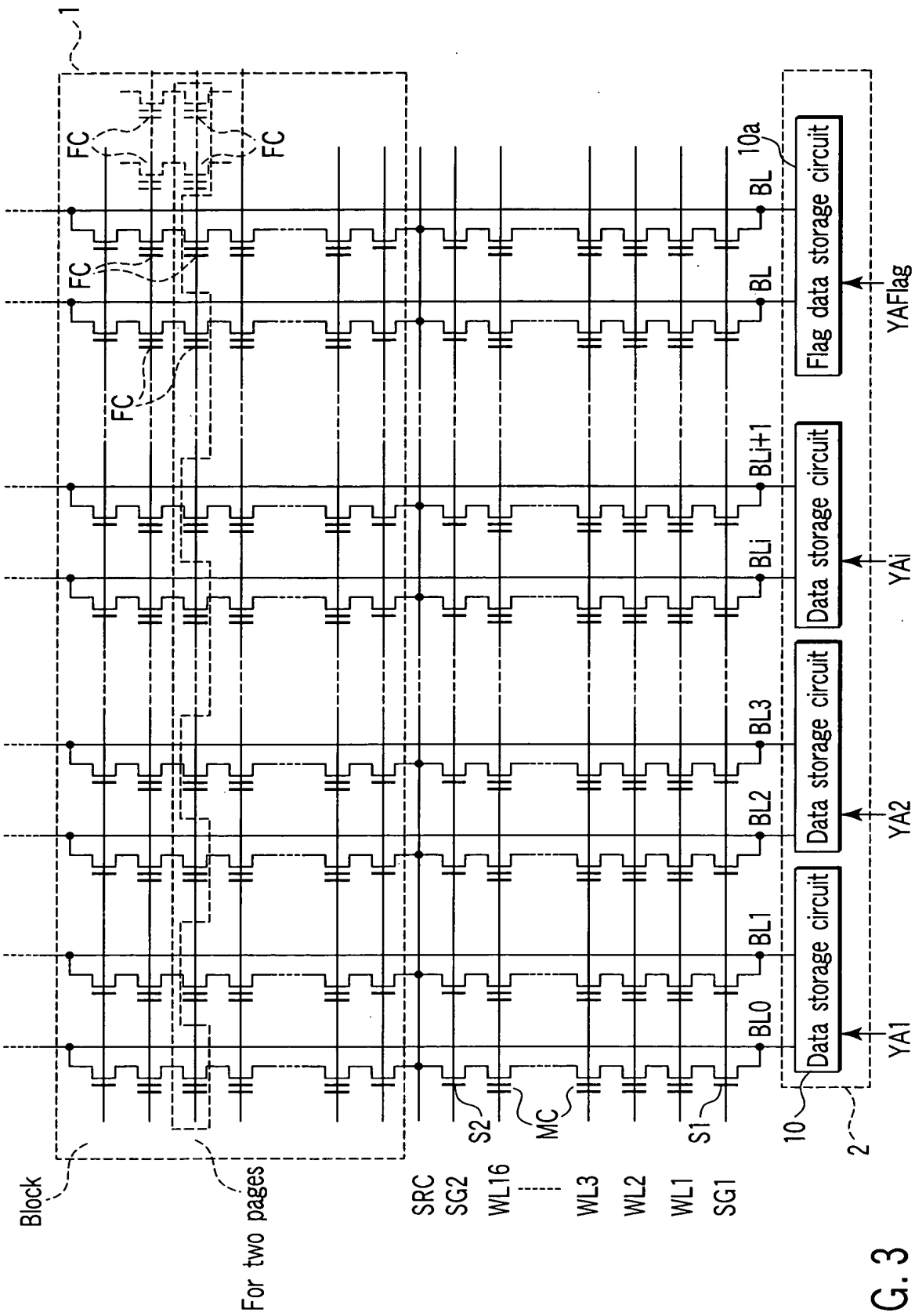


FIG. 3

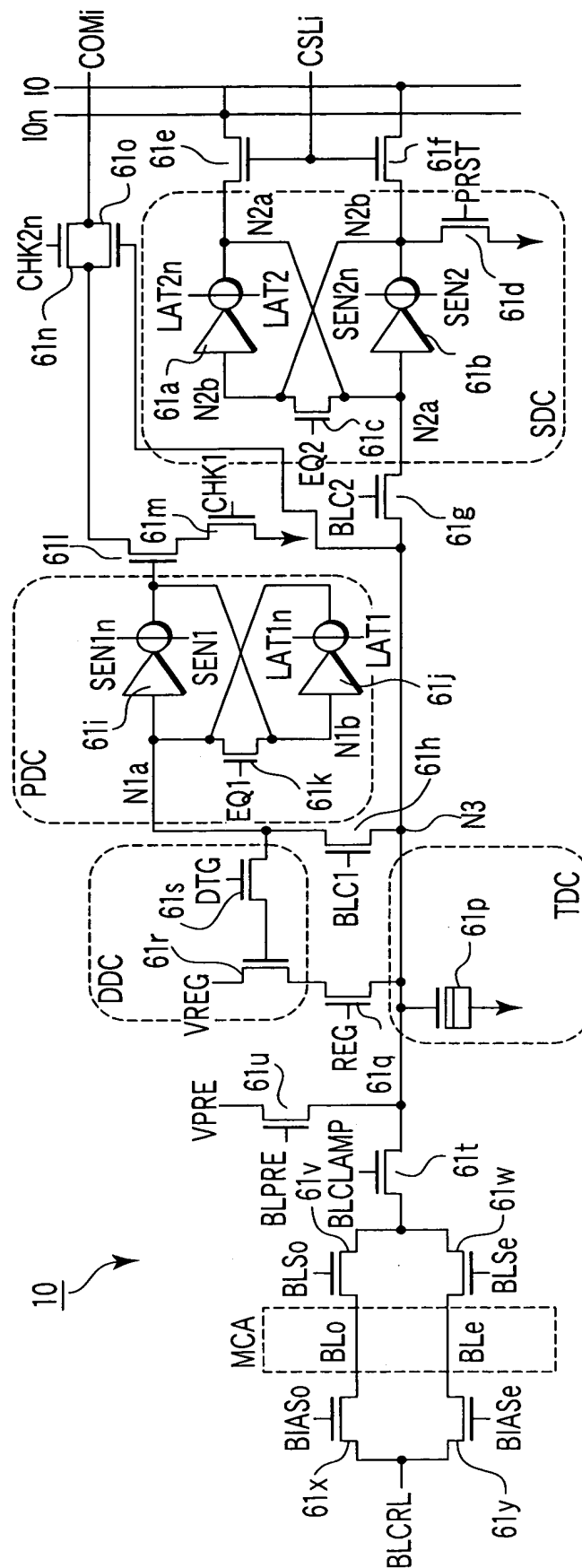


FIG. 6

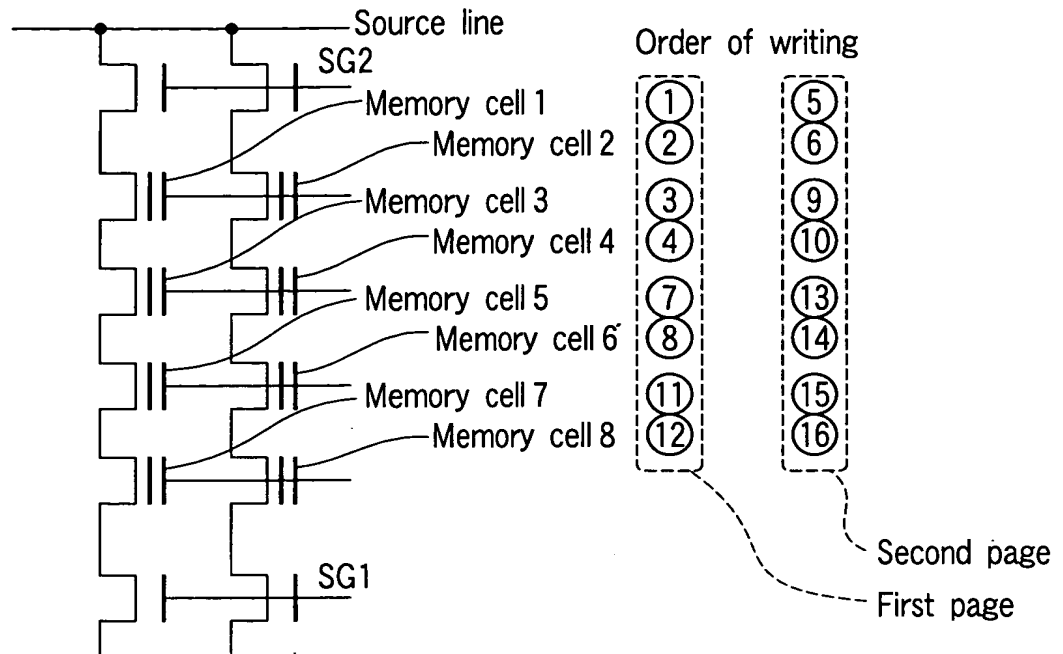


FIG. 7

Writing the first page

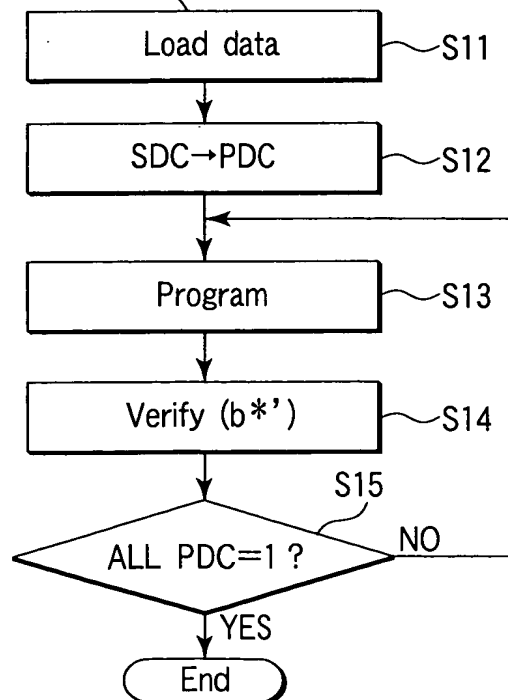


FIG. 8

Writing the second page

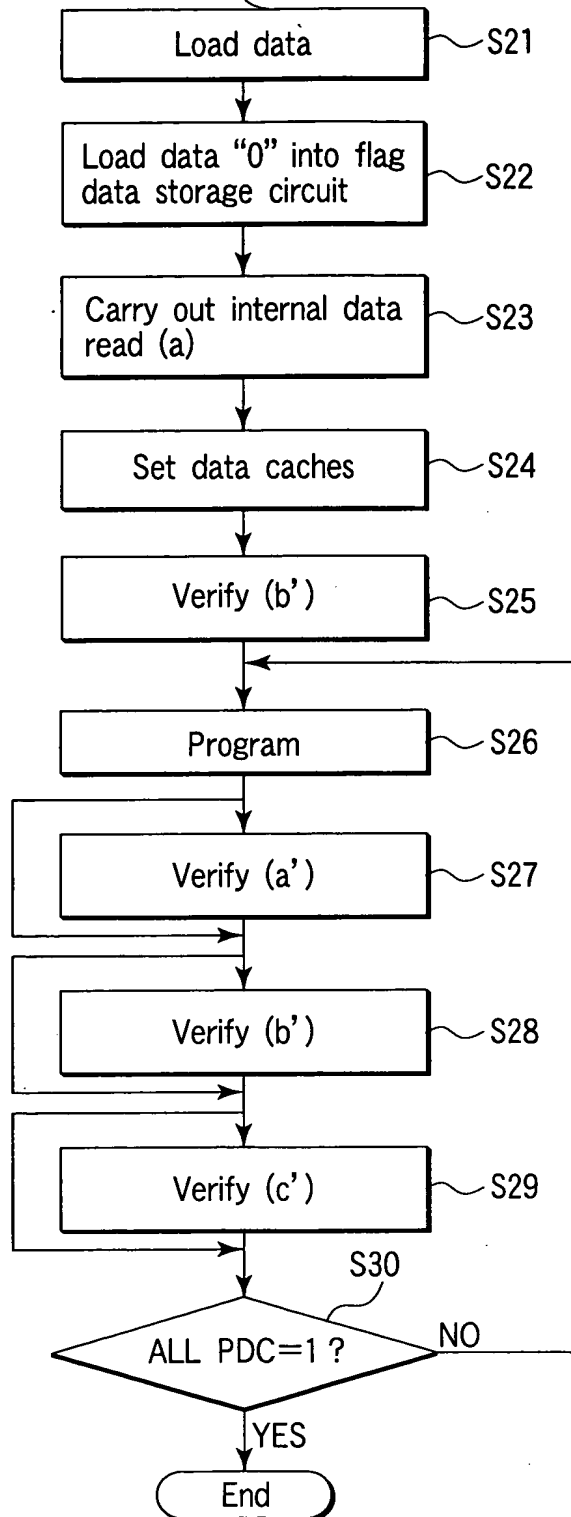


FIG. 9

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 10A

After setting data caches

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected 0 : Write

FIG. 10B

Data cache setting procedure

SDC				DDC				PDC				TDC				
0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	Data in memory cell after writing
1	0	0	1					0	0	1	1					After internal data read
1	0	0	1	0	0	1	1	0	0	1	1					Copy data in PDC into DDC
1	0	0	1	0	0	1	1	1	0	0	1					Copy data in SDC into PDC
1	0	0	1	0	0	1	1	1	0	0	0	1	1	1	1	TDC=H
1	0	0	1	0	0	1	1	1	0	0	1	1	1	0	0	VREG=L, REG=H
1	1	0	0	0	0	1	1	1	0	0	1	1	1	0	0	Copy data in TDC into SDC
1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1	Copy data in PDC into TDC
1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	0	VREG=L, REG=H
1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	0	Copy data in PDC into DDC
1	1	0	0	1	0	0	1	1	0	0	0	1	0	0	0	Copy data in TDC into PDC

FIG.11



1	1	0	0	0	1	0	0	1	1	0	0	0	1	1	1	1	TDC=H
1	1	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0	VREG=L, REG=H
1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	0	Copy data in PDC into DDC
1	1	0	0	0	1	0	0	0	0	1	1	0	0	1	1	0	Copy data in TDC into PDC
1	1	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	TDC=L
1	1	0	0	0	1	0	0	0	0	1	1	0	0	1	0	0	VREG=H, REG=H
1	1	0	0	0	0	1	1	0	0	1	1	0	1	0	0	0	Copy data in PDC into DDC
1	1	0	0	0	0	1	1	0	1	0	0	0	1	0	0	0	Copy data in TDC into PDC
SDC				DDC				PDC				TPC					

FIG. 12

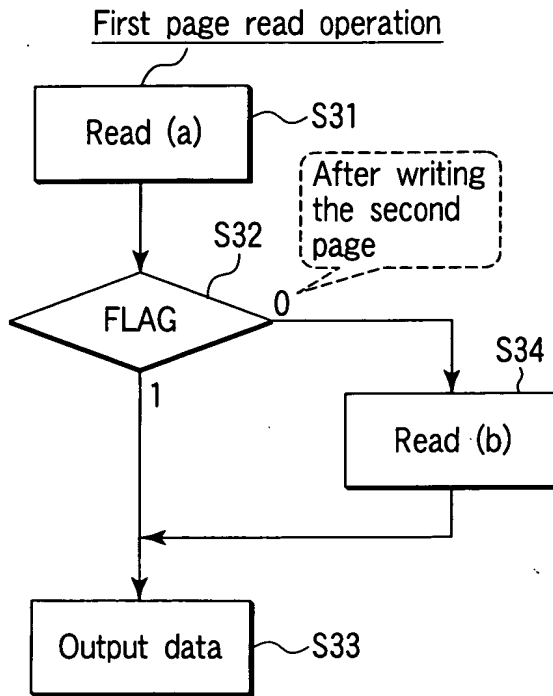


FIG. 13

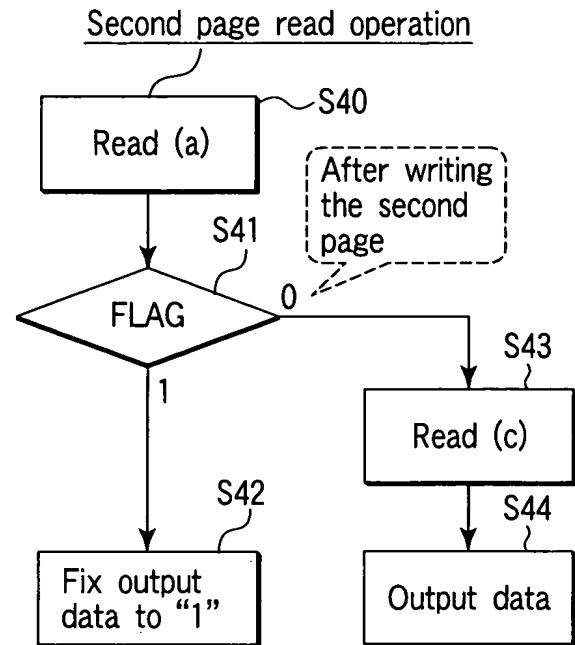


FIG. 15

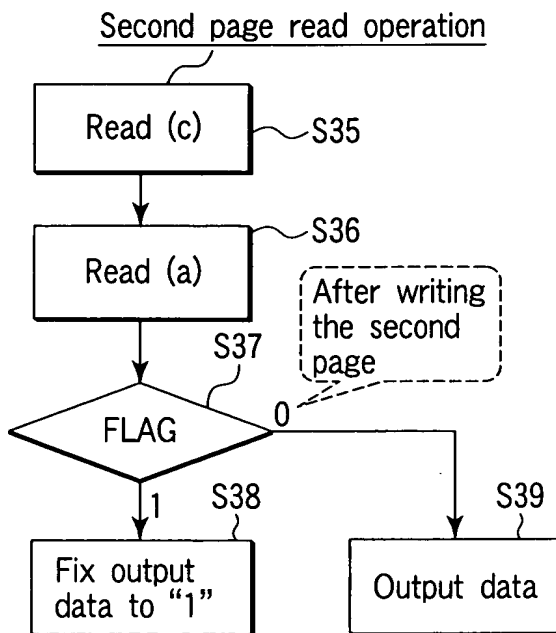


FIG. 14

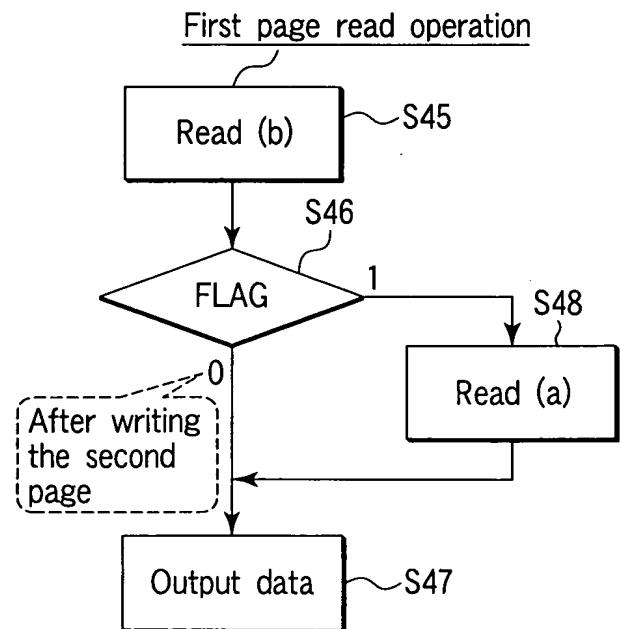


FIG. 16

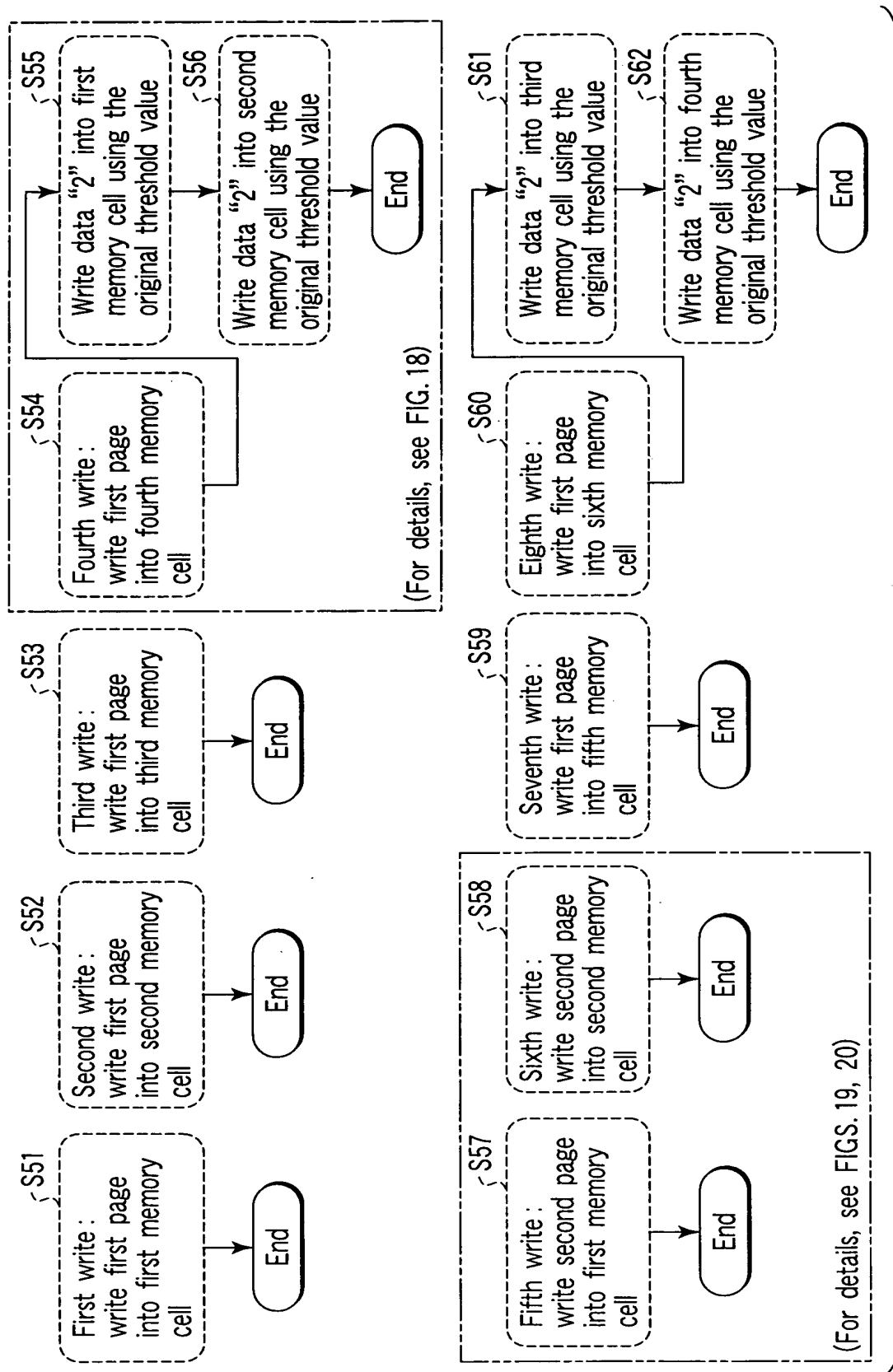


FIG. 17

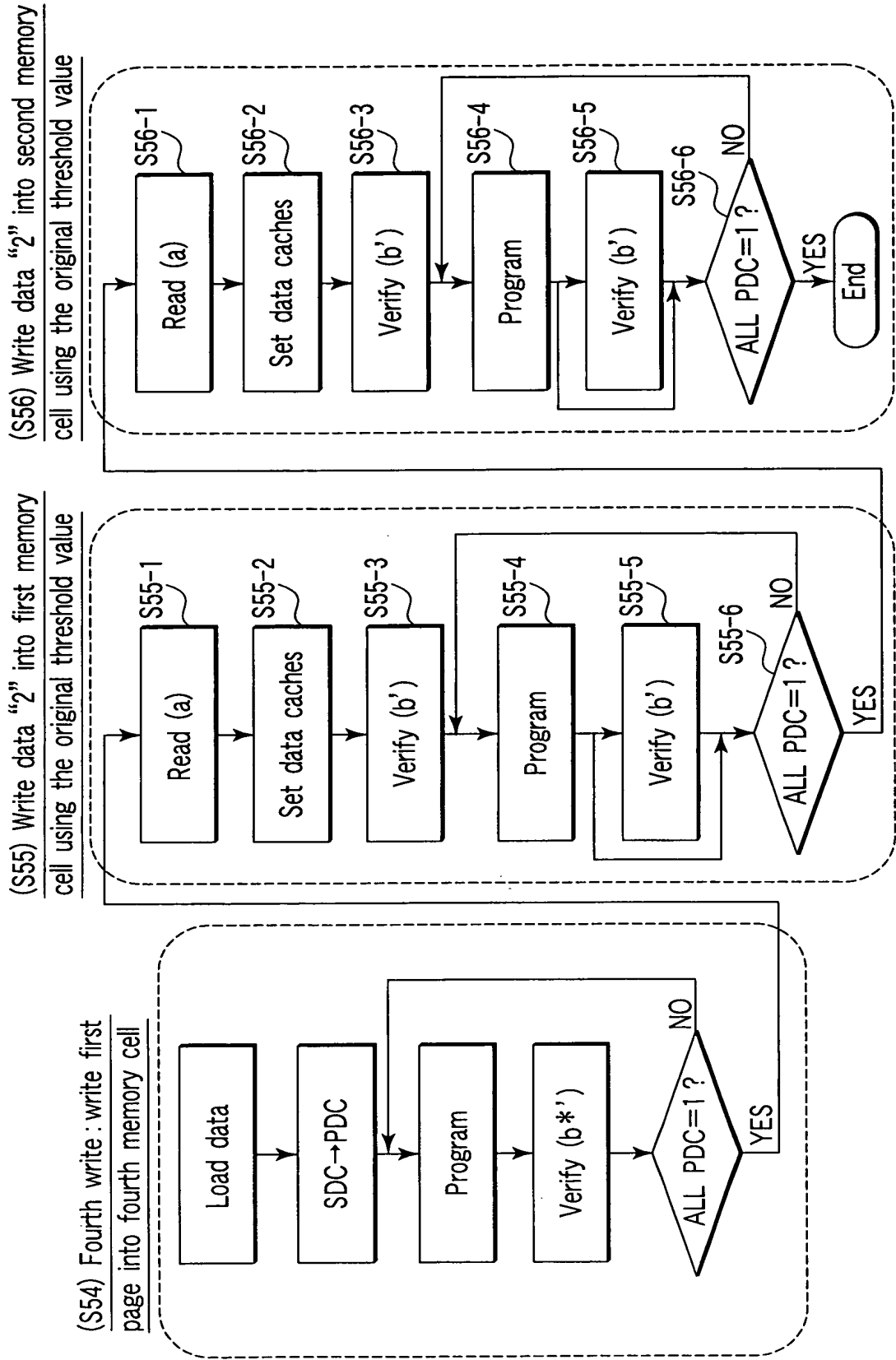


FIG. 18

(S57) Fifth write : write second  
page into first memory cell

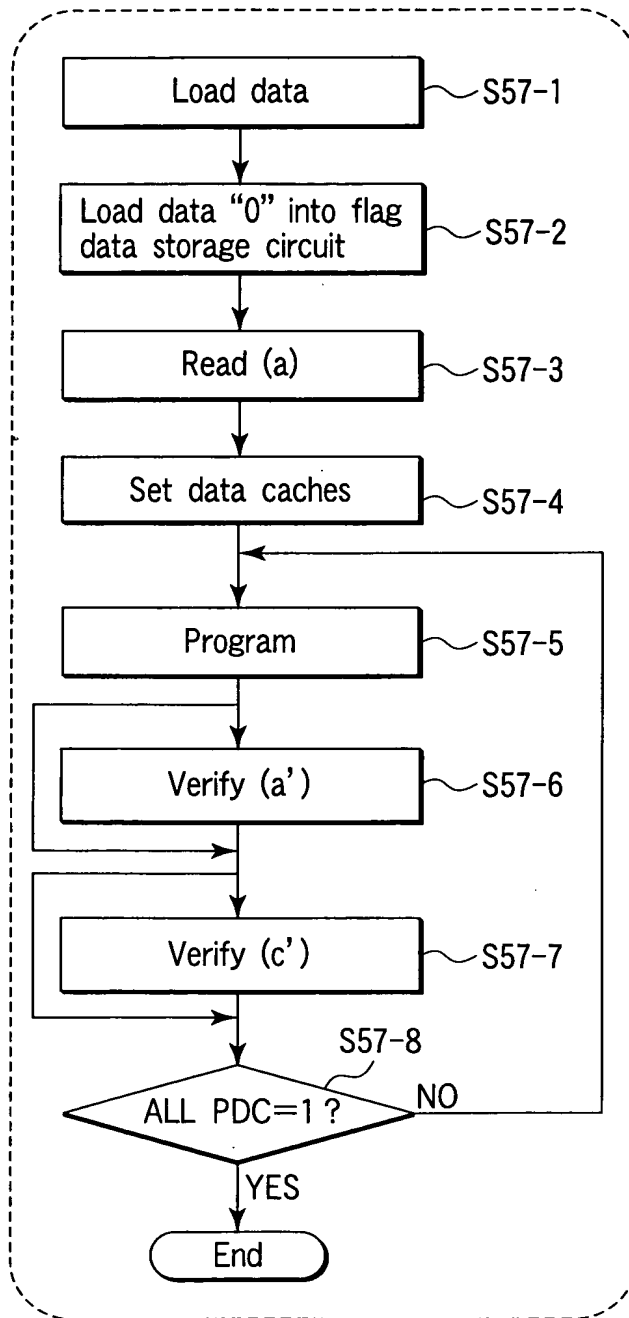


FIG. 19

(S58) Sixth write : write second  
page into second memory cell

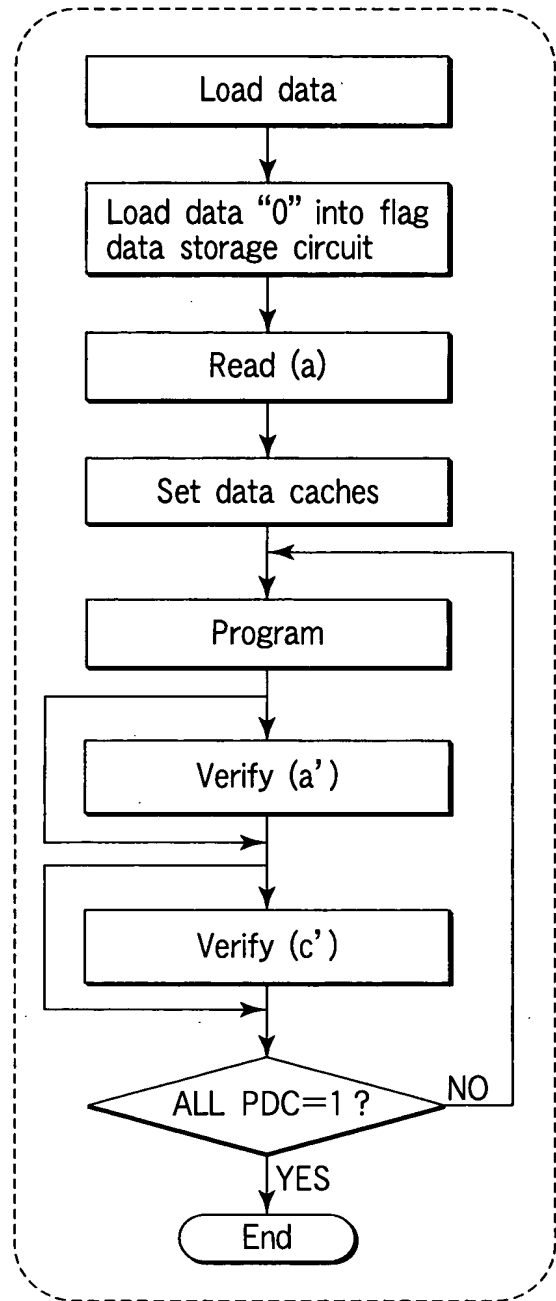


FIG. 20

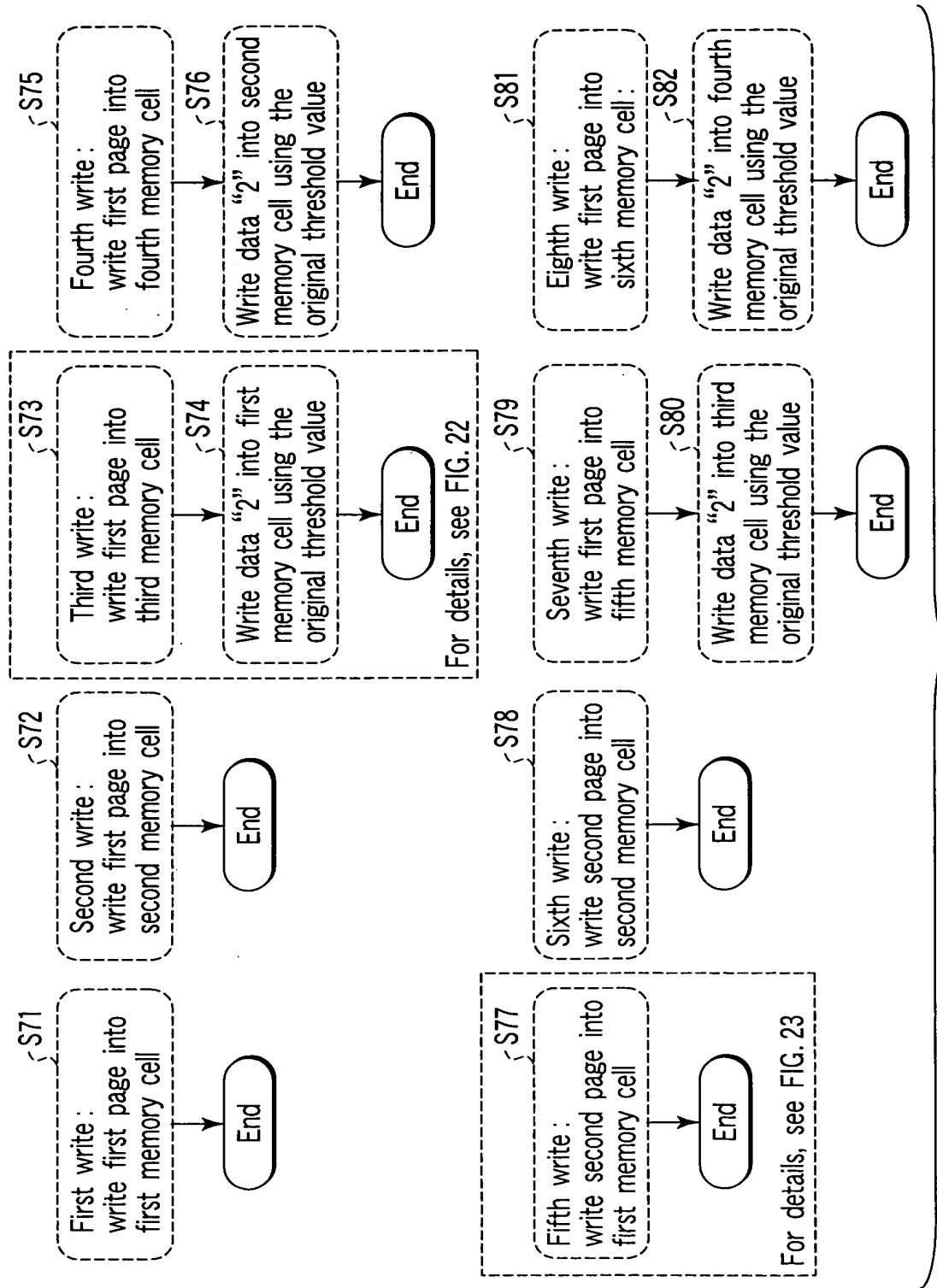
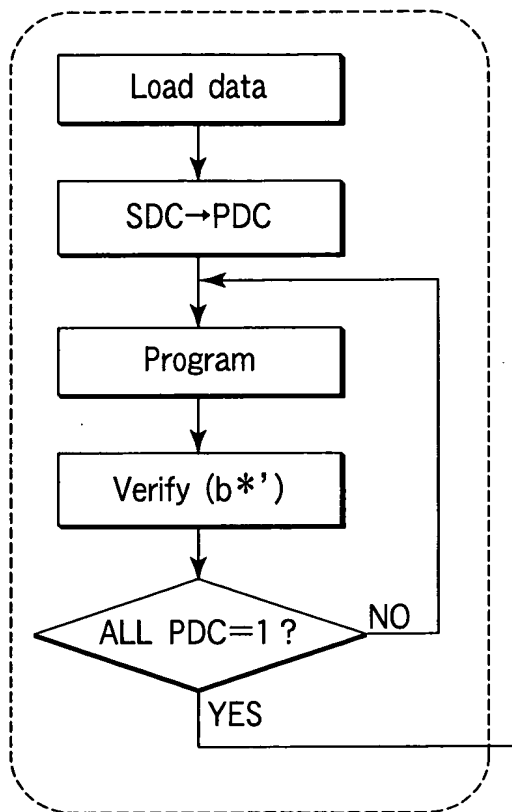


FIG. 21

(S73) Third write : write first  
page into third memory cell



(S74) Write data "2" into first memory  
cell using the original threshold value

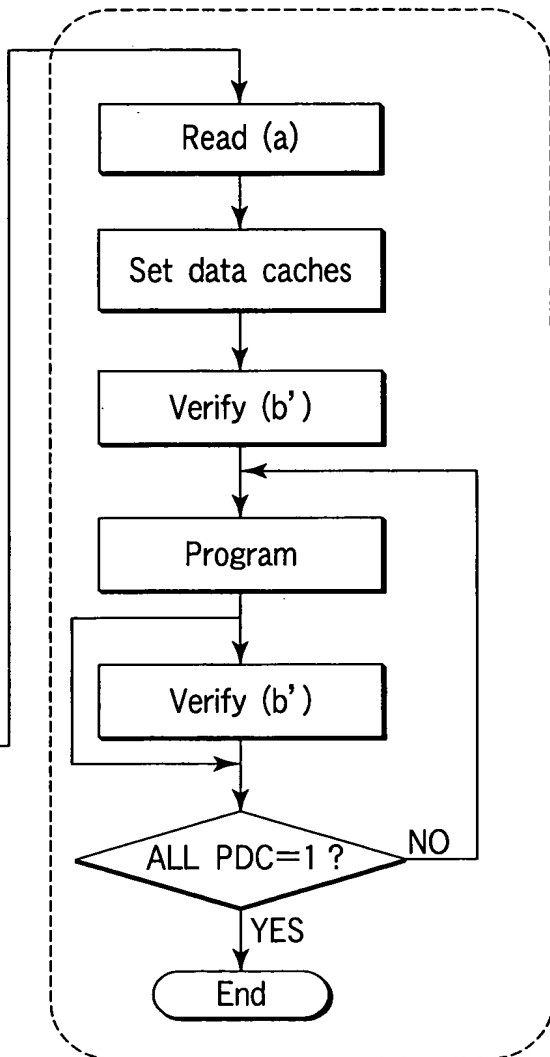


FIG. 22

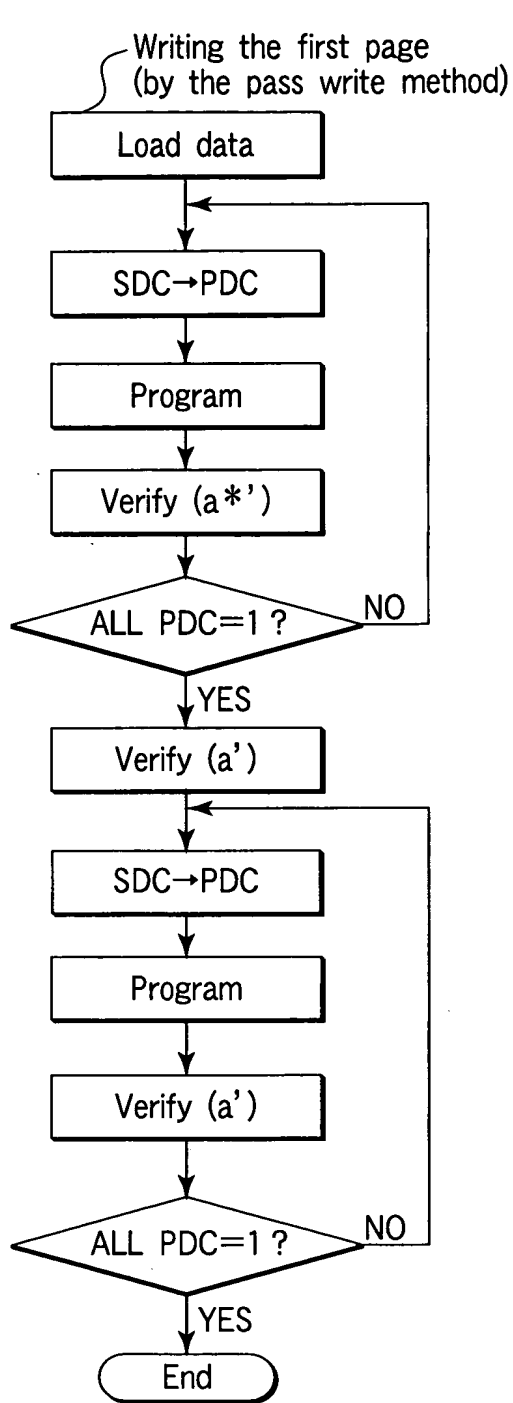


FIG. 23A

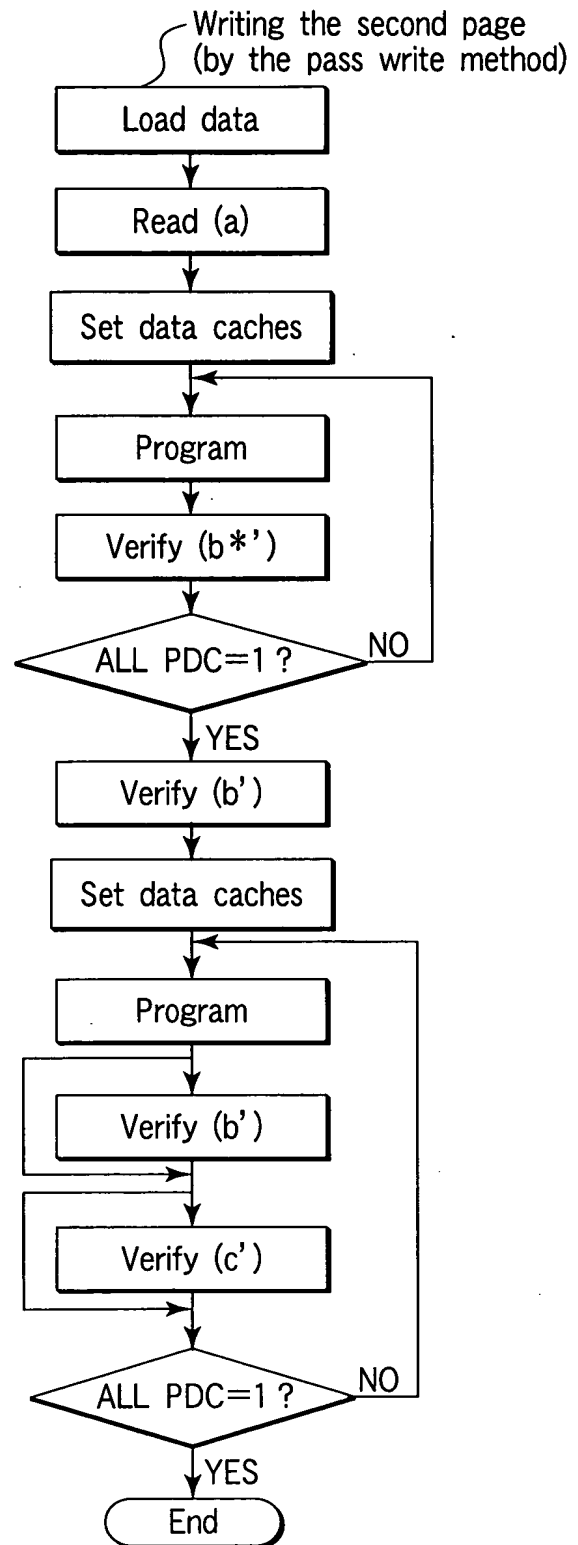


FIG. 23B



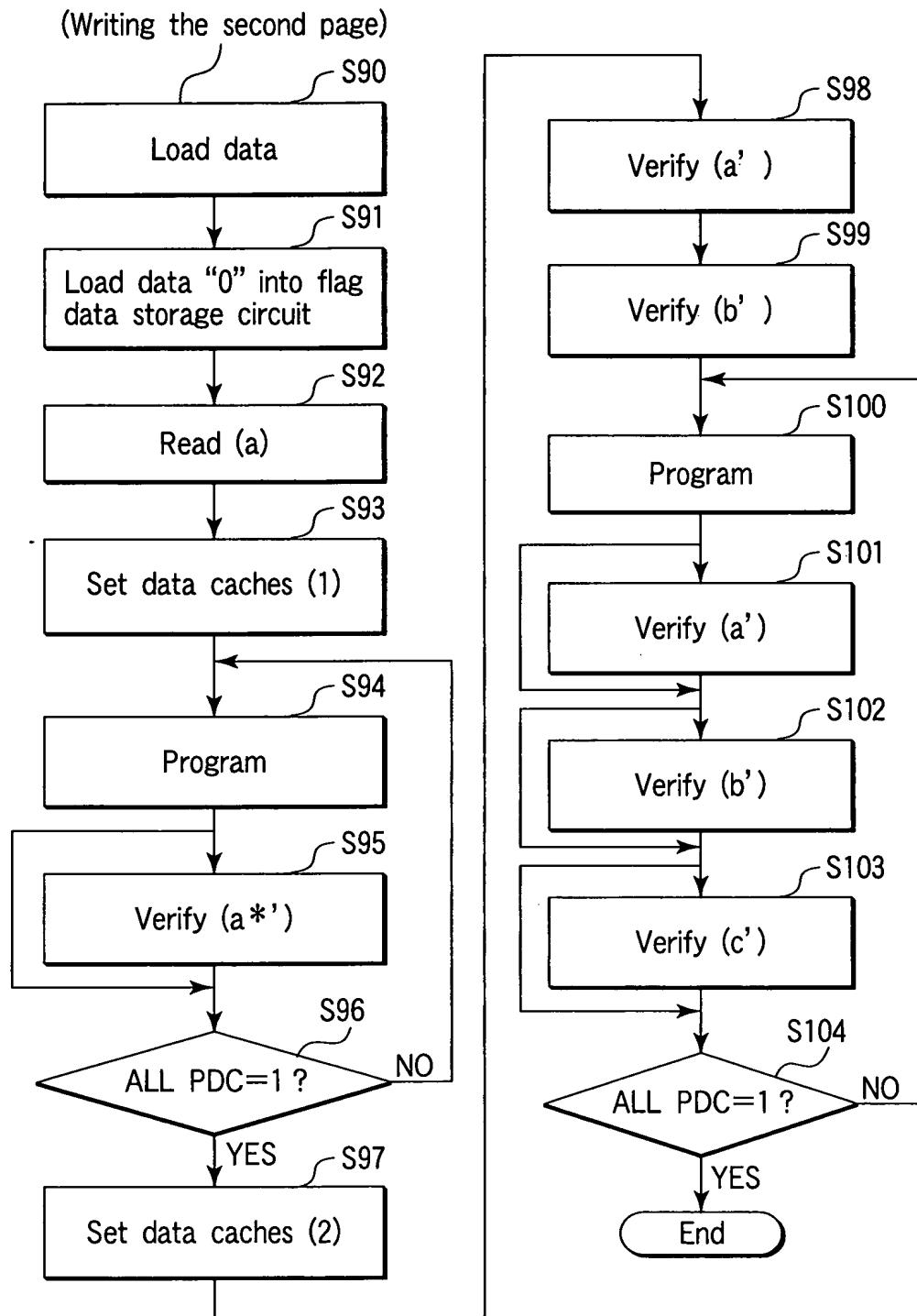


FIG. 24

Data cache setting 1

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	
DDC	0	0	1	1	
PDC	1	0	1	1	1 : Write unselected 0 : Write

FIG. 25

(Writing the second page)

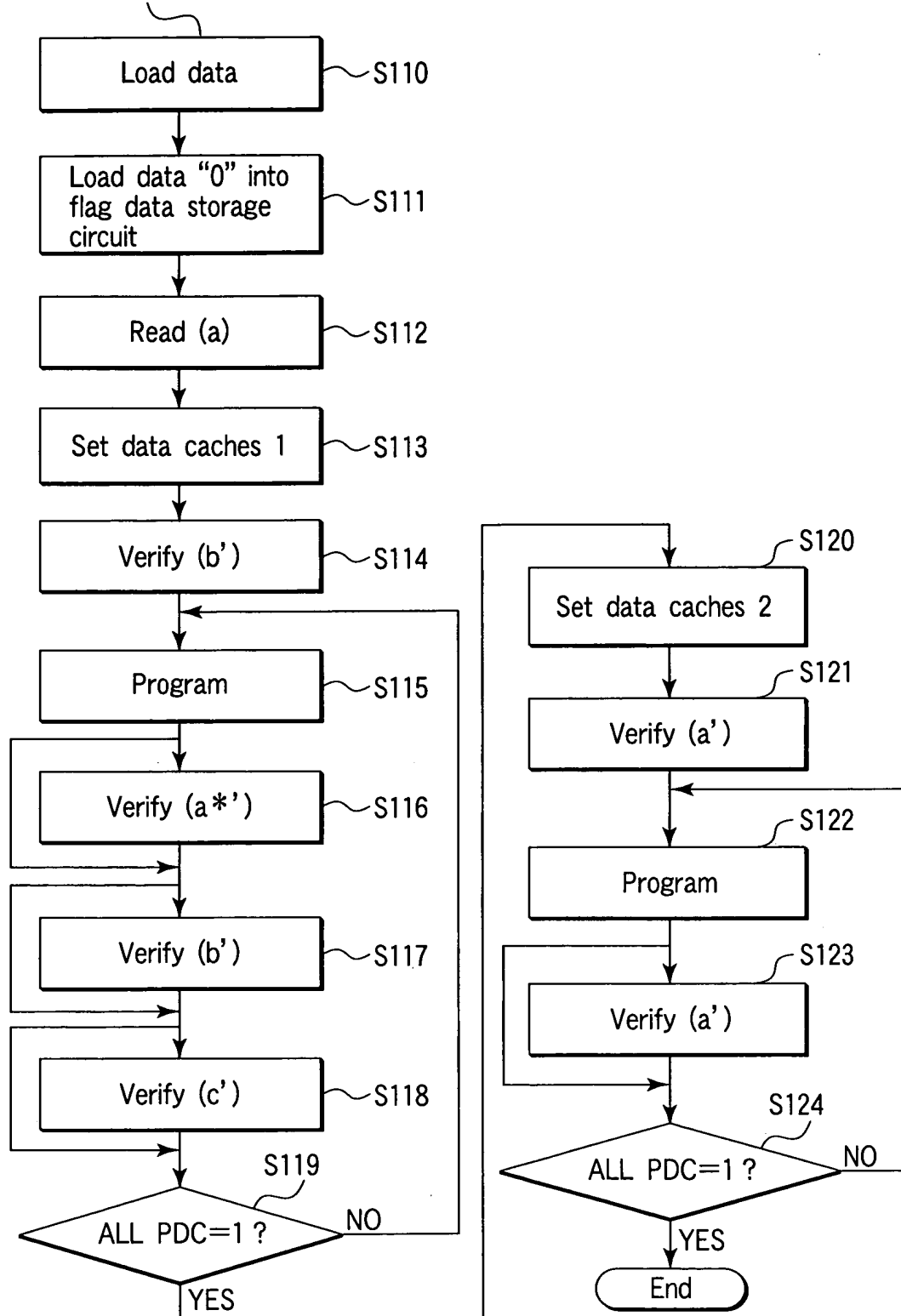


FIG. 26

Data cache setting 1

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	0	0	Used far charging in verifying memory cell data 1
DDC	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected 0 : Write

FIG. 27A

Data cache setting 2

	Data in memory cell after writing				
	0	1	2	3	
PDC	1	0	1	1	1 : Write unselected 0 : Write

FIG. 27B

(Writing the second page)

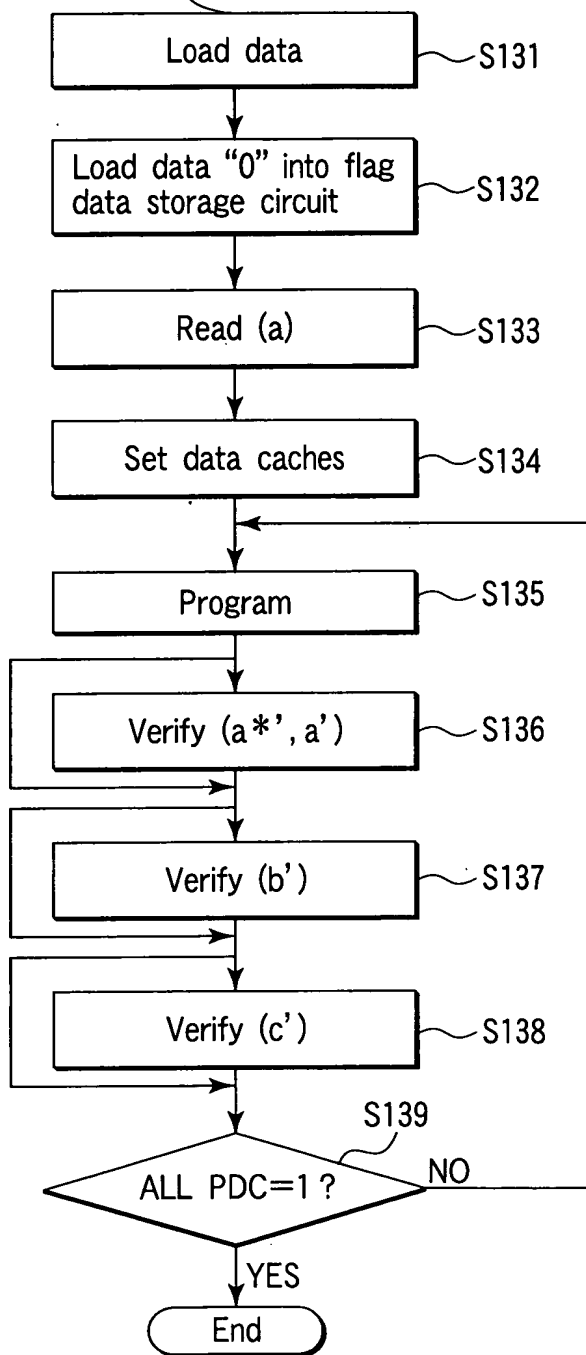


FIG. 28

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 29A

After data cache setting

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	0	0	1 : Write unselected 0 : Write

FIG. 29B

Precharge bit line on the basis of the data in DDC

	Data in memory cell after writing			
	0	1	2	3
Bit line	Vdd	F (Vss)	Vdd	Vdd

FIG. 30A

With BLC1 = Vclamp, connect PDC to bit line

	Data in memory cell after writing			
	0	1	2	3
Bit line	Vdd	0/Inter-mediate	0	0

FIG. 30B

During program recovery, transfer data in PDC to DCC, invert data in DCC, and transfer the inverted data to PDC

	Data in memory cell after writing			
	0	1	2	3
SDC	0	1	1	0
DDC	1	0/1	0	0
PDC	0	1	0	0

Used for charging in verifying memory cell data 2

1 : Write unselected 0 : Write

Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 30C

Verify (a)  
Charge bit line on the basis of data in PDC  
Discharge bit line at a potential of  $WL = a^*$   
Invert data in PDC while discharging bit line

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1 : Write unselected 0 : Write
PDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 31A

Load the potential of bit line into TDC  
With  $V_{REG} = H$  and  $REG = H$ , make TDC 1 when dynamic data is 1  
Transfer data in PDC to DDC and data in TDC to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	0	1	User for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	1	1	1 : Write unselected 0 : Write

FIG. 31B



With WL = a', discharge bit line  
 With VREG = H and REG = H, set 1 in TDC when dynamic data is 1  
 Transfer data in PDC to DDC  
 Transfer data in TDC to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1 : Write unselected 0 : Write
PDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 32A

Transfer data in DDC to PDC  
 Then, transfer data in PDC to DDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	0	0	1 : Write unselected 0 : Write

FIG. 32B

With memory cell data 1, all of the writing with verify (a\*) is completed  
(the writing with verify (a') might nat be completed)

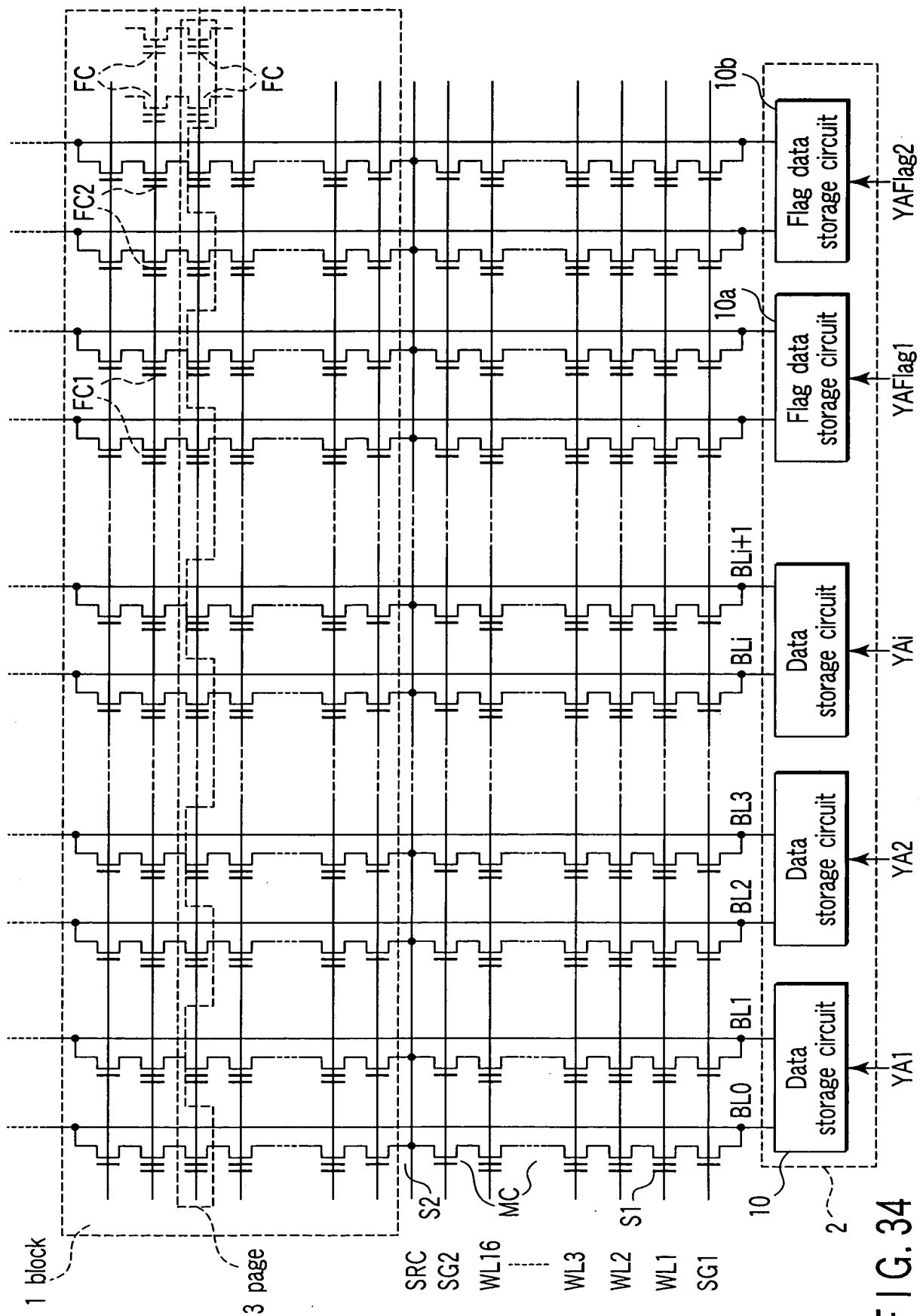
	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used far charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	1	0	0	1 : Write unselected 0 : Write

F I G. 33A

With memory cell data 1, all of the writing with verify (a') is completed  
(the writing with verify (a') might not be completed)

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	1	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	1	0	0	1 : Write unselected 0 : Write

F I G. 33B



(After writing first page and before writing second page)

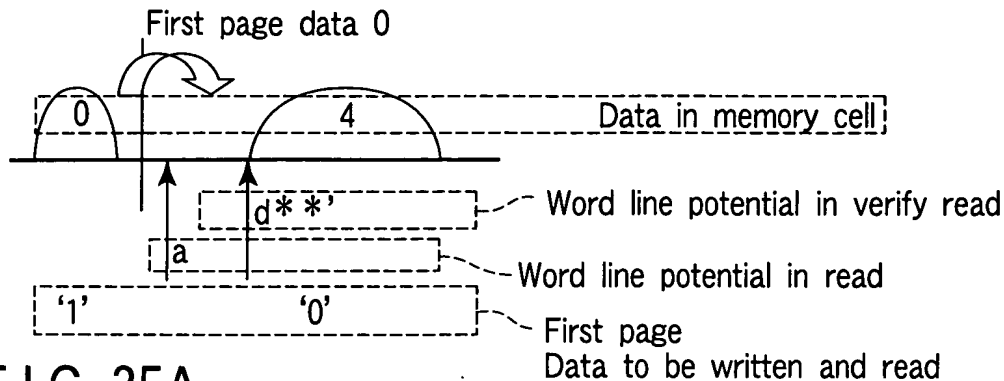


FIG. 35A

(After writing first page, before writing second page,  
 and after writing adjacent cells of first page)

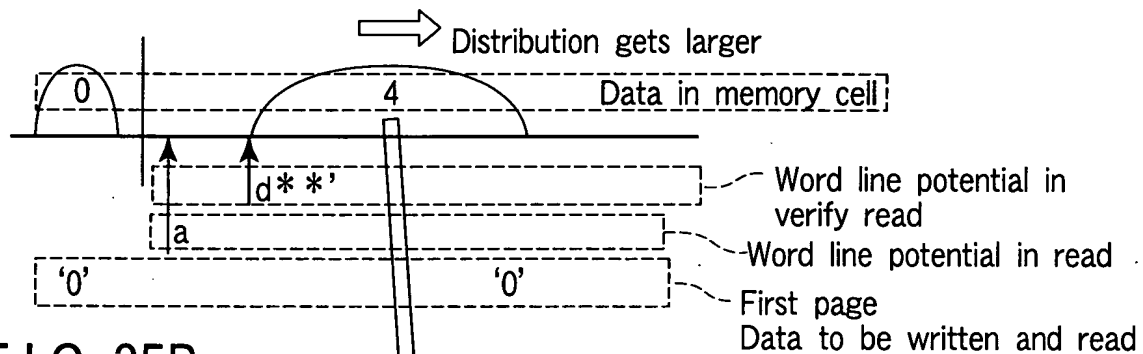


FIG. 35B

After writing second page, before writing third page,  
 and after writing adjacent cells of second page

With first page data 1,  
 second page data 0 is  
 obtained

With first page data 0,  
 second page data 1 is  
 obtained

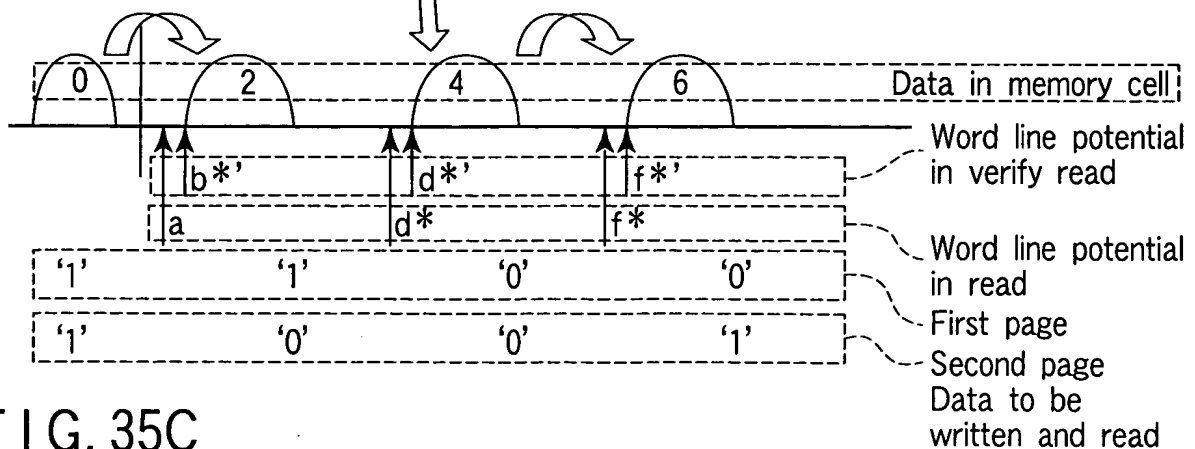


FIG. 35C

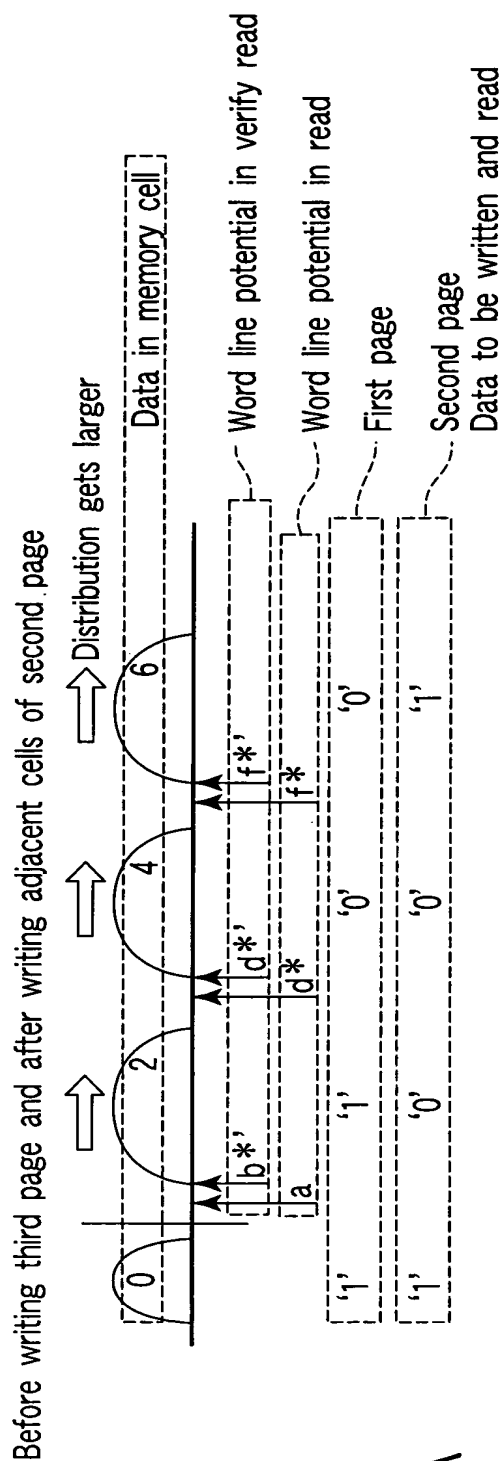
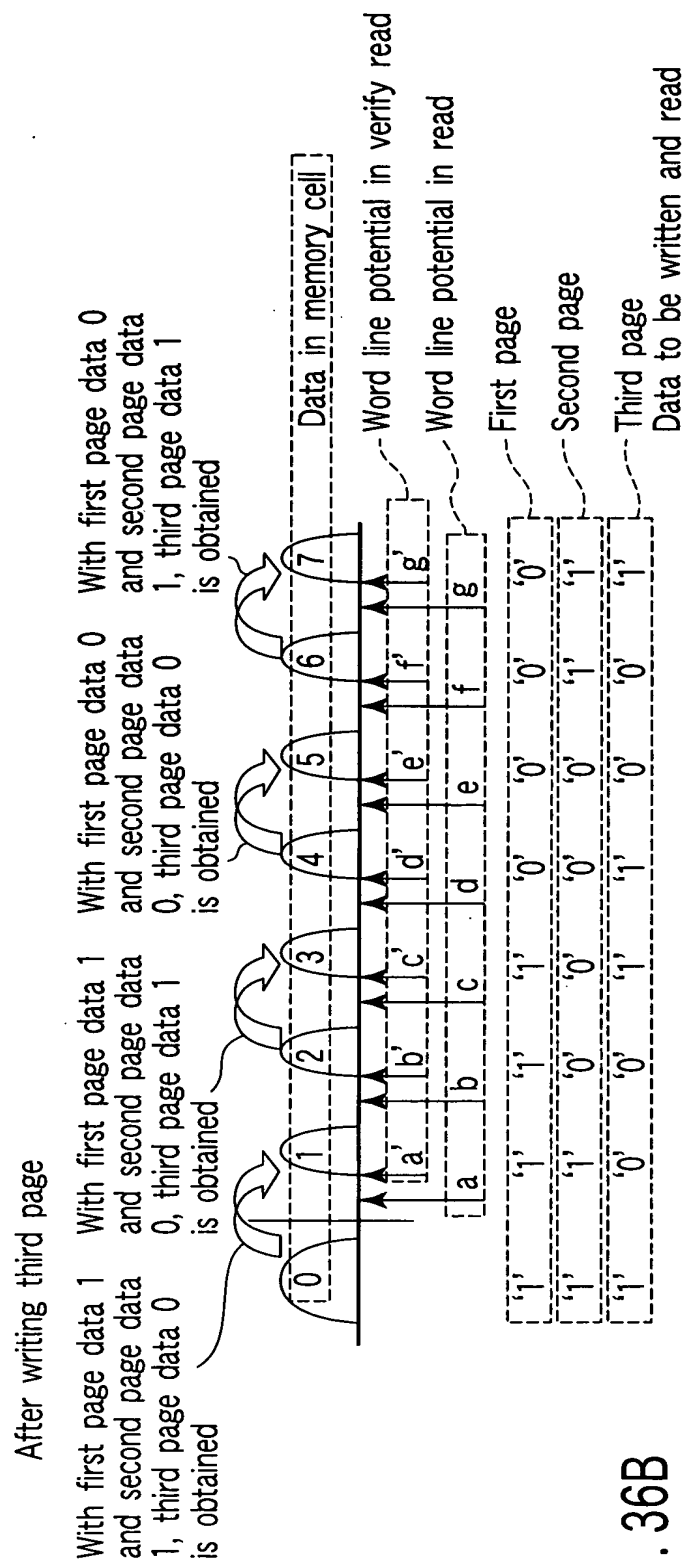


FIG. 36A



F I G. 36B

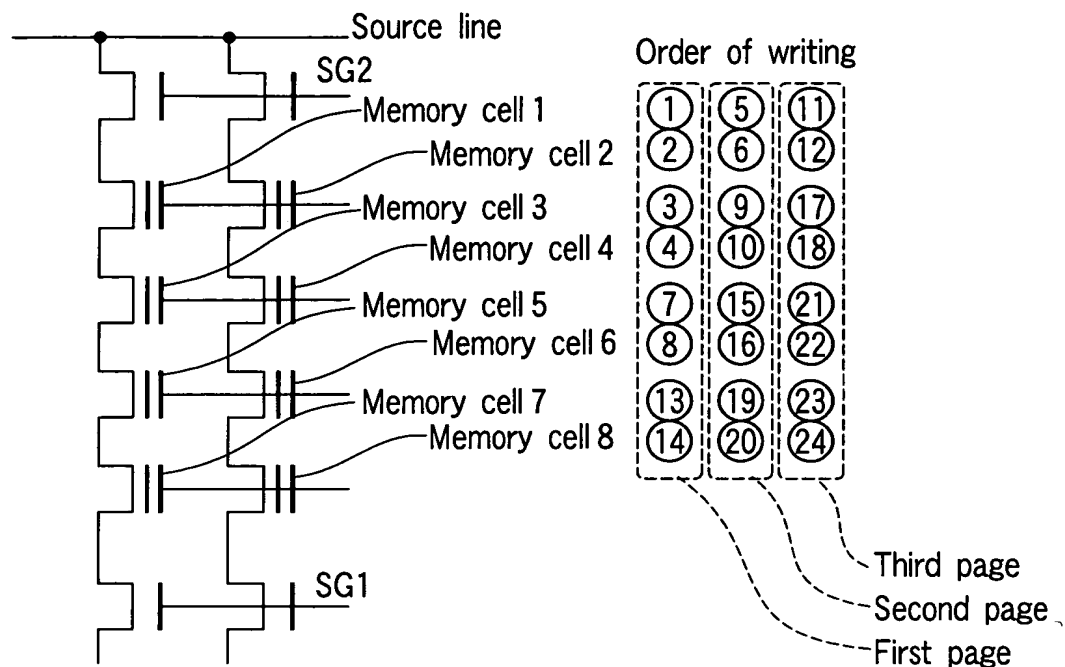


FIG. 37A

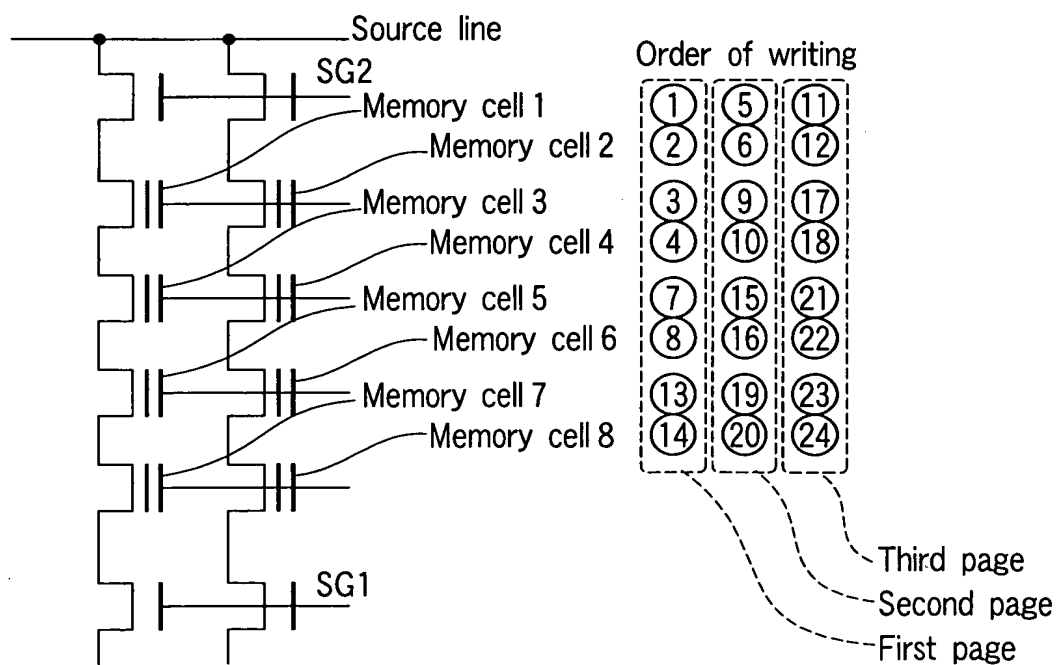


FIG. 37B

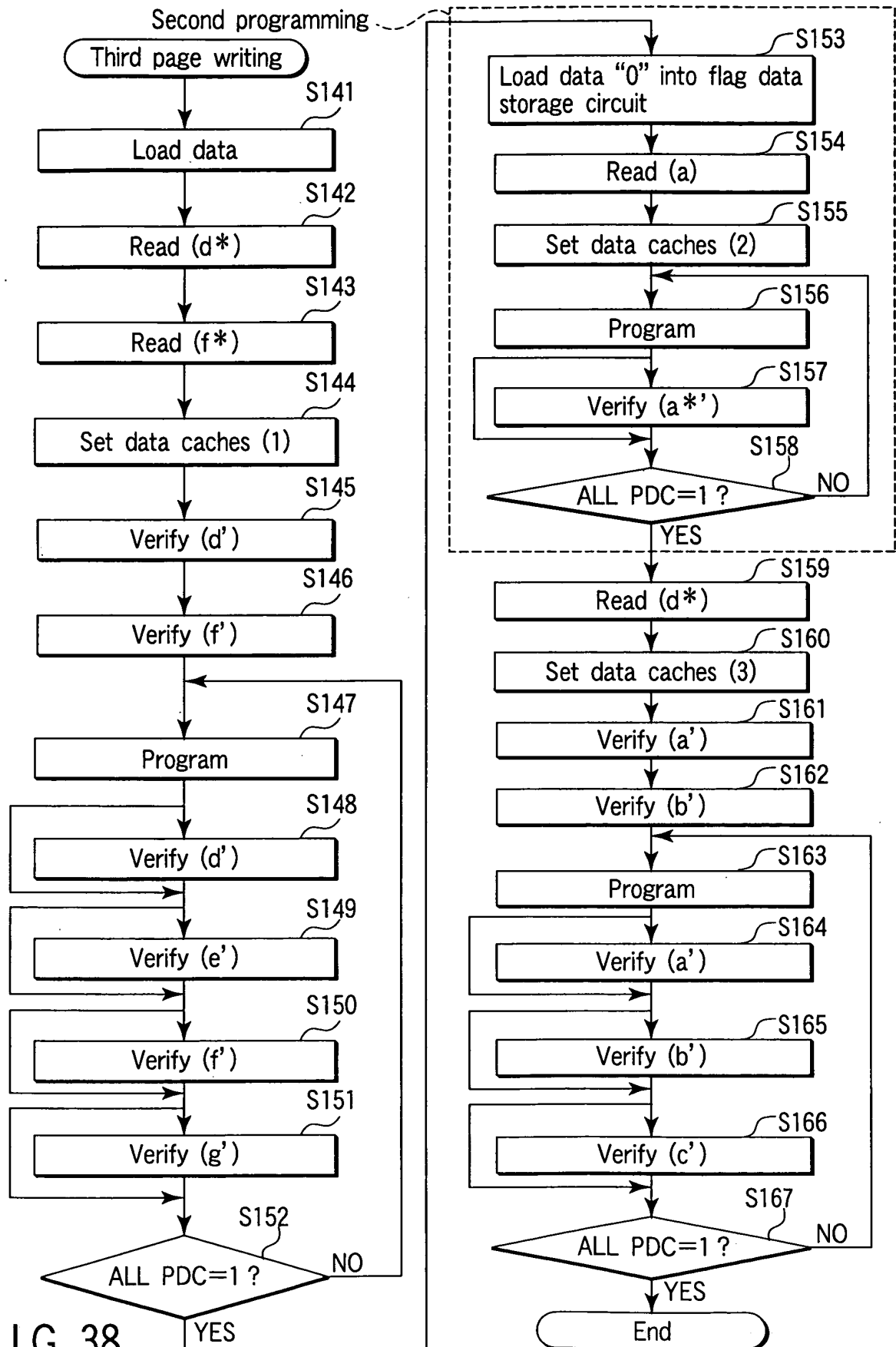


FIG. 38

After third page data load internal read 1

	Data in memory cell after writing								
	0	1	2	3	4	5	6	7	
SDC	1	0	0	1	1	0	0	1	Data to be written and read inputted from the outside world
DDC	0	0	0	0	0	0	1	1	Data to be read by internal read
PDC	0	0	0	0	1	1	1	1	Data to be read by internal read

FIG. 39A

After third page data cache setting 1

	Data in memory cell after writing								
	0	1	2	3	4	5	6		7
SDC	1	1	1	1	1	1	0	0	Used far charging in verifying memory cell data items 5, 4
DDC	0	1	1	0	0	1	1	0	Used for charging in verifying memory cell data 6 Forced to be at VSS in verifying memory cell data 4
PDC	1	1	1	1	0	0	0	0	1 : Write unselected 0 : Write

FIG. 39B



After third page data cache setting 2

	Data in memory cell after writing								
	0	1	2	3	4	5	6		7
	0	1	2	3	4	5	6	7	
SDC	1	1	0	0	0	0	0	0	
DDC	0	1	1	0	0	1	1	0	
PDC	1	0	1	1	1	1	1	1	1 : Write unselected 0 : Write

FIG. 40A

After third page data cache setting 3

	Data in memory cell after writing								
	0	1	2	3	4	5	6	7	
SDC	1	1	0	0	0	0	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	1	0	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1	1	1	1	1 : Write unselected 0 : Write

FIG. 40B

First page read operation

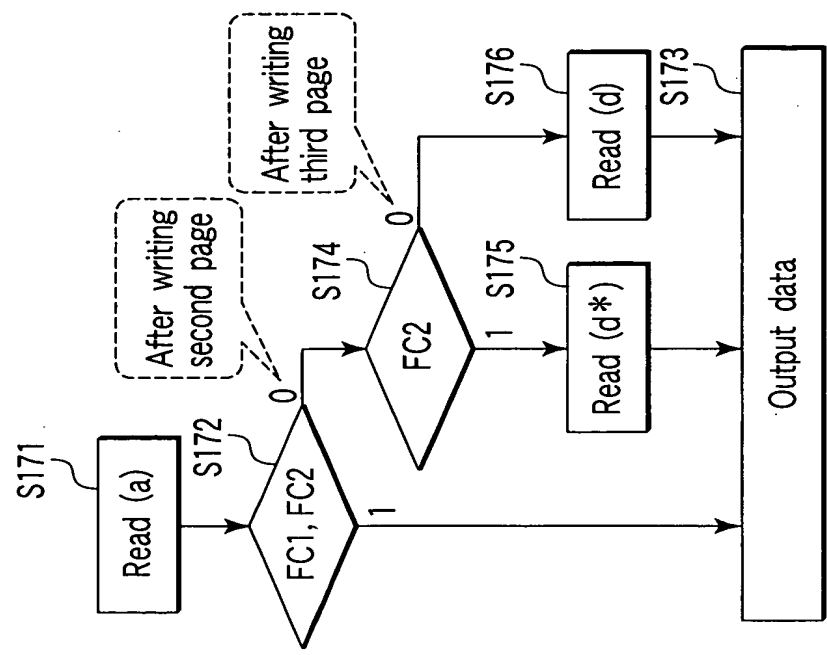


FIG. 41A

Second page read operation

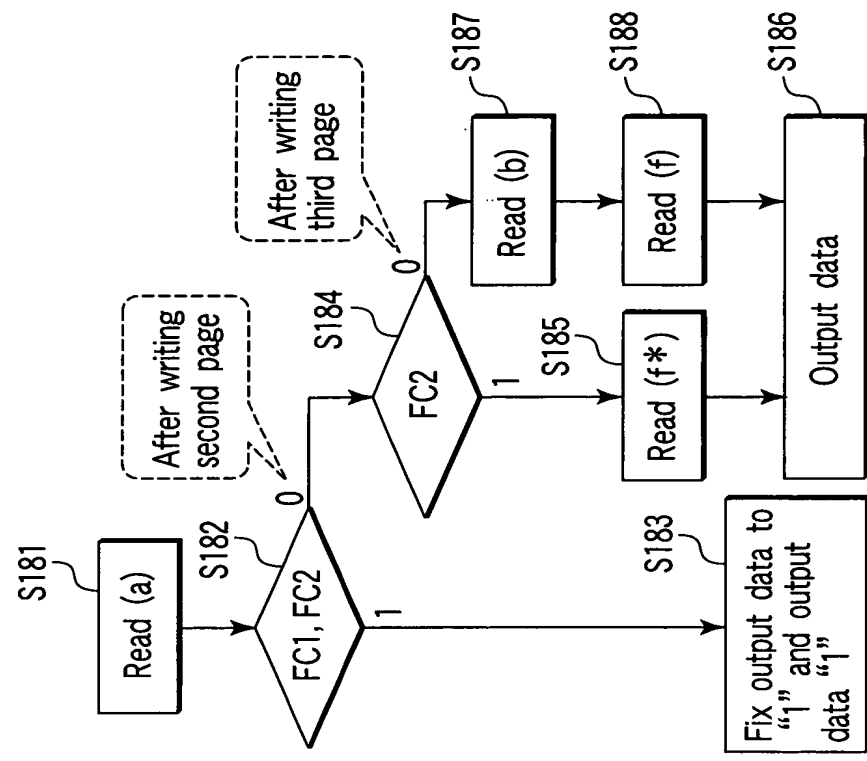


FIG. 41B

Third page read operation

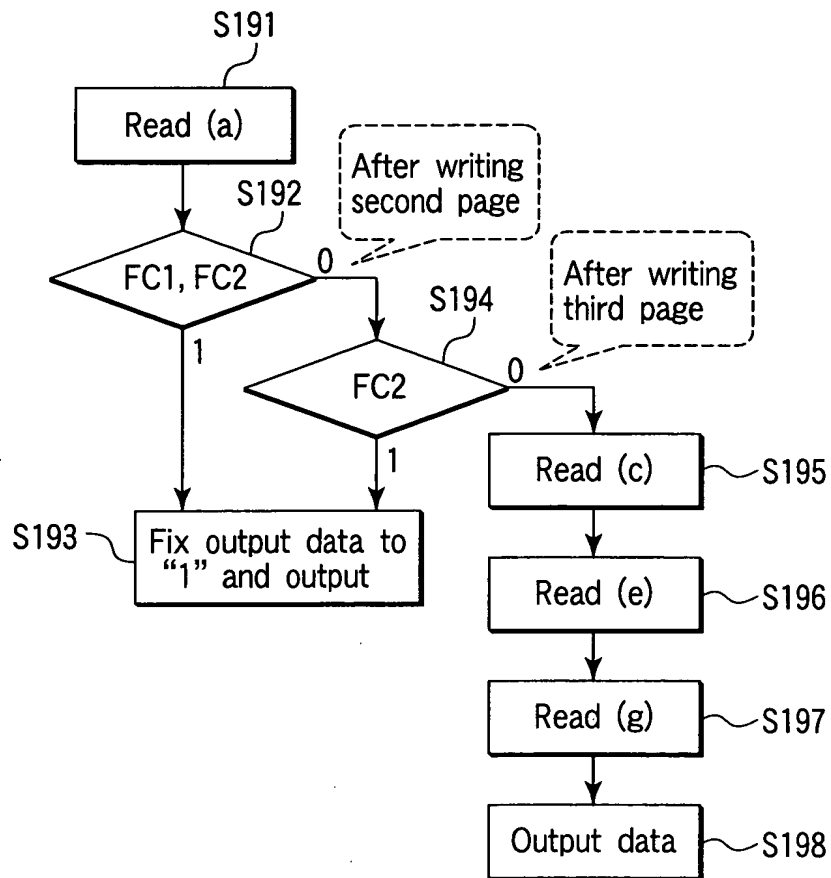


FIG. 42

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 43A

After setting data caches

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	0	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected, 0 : Write

FIG. 43B

Verify (a\*)  
 Charge bit line on the basis of data in SDC  
 Discharge bit line at a potential of WL=a\*'

	Data in memory cell after writing			
	0	1	2	3
SDC	1	1	0	0
DDC	0	0	1	0
PDC	1	0	0	0
				Used for charging in verifying memory cell data 1
				Used for charging in verifying memory cell data 2
				1 : Write unselected, 0 : Write

FIG. 44A

Set Vdd in TDC and transfer the potential of bit line to TDC when BLCLAMP is H  
 With VREG=H, REG=H, make TDC 1 when dynamic data is 1  
 Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing			
	0	1	2	3
SDC	1	1	0	0
DDC	1	0	0	0
PDC	0	0/1	1	0
				Used for charging in verifying memory cell data 1
				1 : Write unselected, 0 : Write
				Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds a*' $\rightarrow$ 1

FIG. 44B

Discharge bit line at a potential of  $WL=a'$   
 Set  $V_{dd}$  in TDC and transfer the potential of bit line to TDC when  $BLCLAMP$  is H  
 With  $V_{REG}=H$ ,  $REG=H$ , make TDC 1 when dynamic data is 1  
 Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing					
	0	1pass	1fail	2	3	
SDC	1	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	0/1	1	0	Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds $a^* \rightarrow 1$
PDC	1	1	0	0	0	1 : Write unselected, 0 : Write

FIG. 45A

Verify (b')

Charge bit line on the basis of data in DDC

Discharge bit line at a potential of WL=b'

Transfer data in DDC to TDC, PDC to DDC and TDC to PDC during the discharge

Set Vdd in TDC and transfer the potential of bit line to TDC when BLCLAMP is H

With VREG=H, REG=H, make TDC 1 when dynamic data is 1

Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing				
	0	1	2fail	2pass	3
SDC	1	1	0	0	0
DDC	0	0/1	1	1	0
PDC	1	0	0	1	0
					Used for charging in verifying memory cell data 1
					Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds a* → 1
					1 : Write unselected, 0 : Write

FIG. 45B

Verify (c)  
Charge bit line  
Discharge bit line at a potential of WL=c'  
Transfer data in DDC to TDC, PDC to DDC and TDC to PDC during the discharge  
Set Vdd in TDC and transfer the potential of bit line to TDC when BLCLAMP is H  
With VREG=H, REG=H, make TDC 1 when dynamic data is 1  
Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing					
	0	1	2	3fail	3pass	
SDC	1	1	0	0	0	Used for charging in verifying memory cell data 1
DDC	0	0/1	1	0	0	Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds $a' \rightarrow 1$
PDC	1	0	0	0	1	1 : Write unselected, 0 : Write

FIG. 46



Before writing the second page

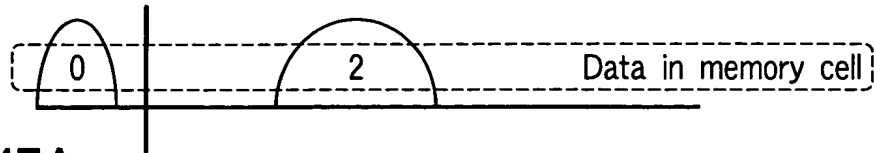


FIG. 47A

After writing the second page

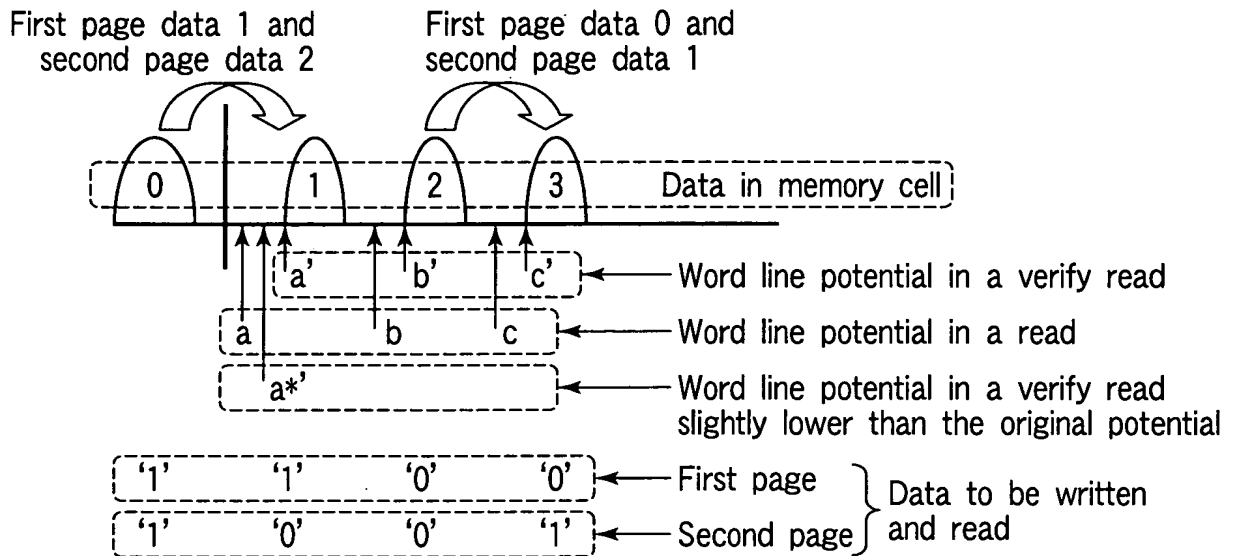


FIG. 47B

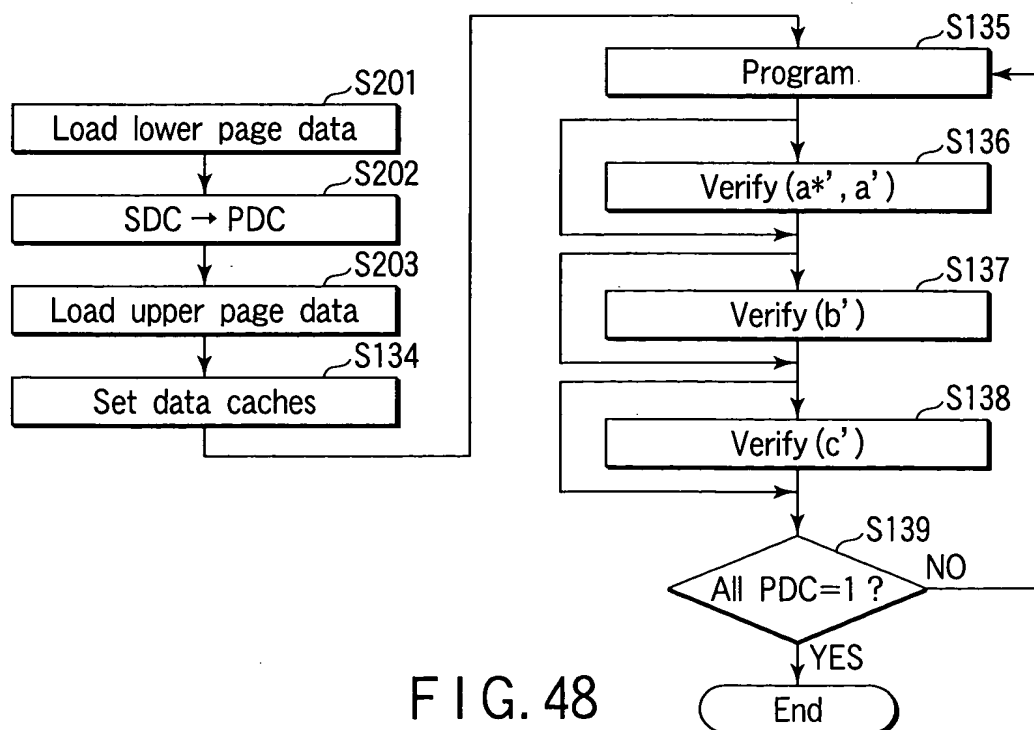


FIG. 48

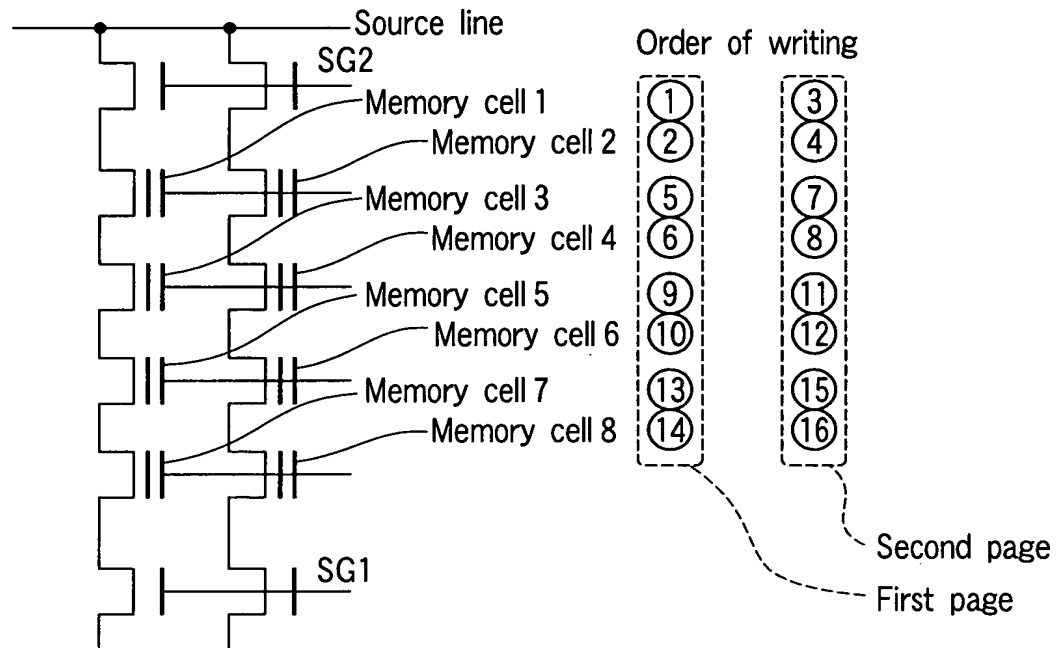


FIG. 49

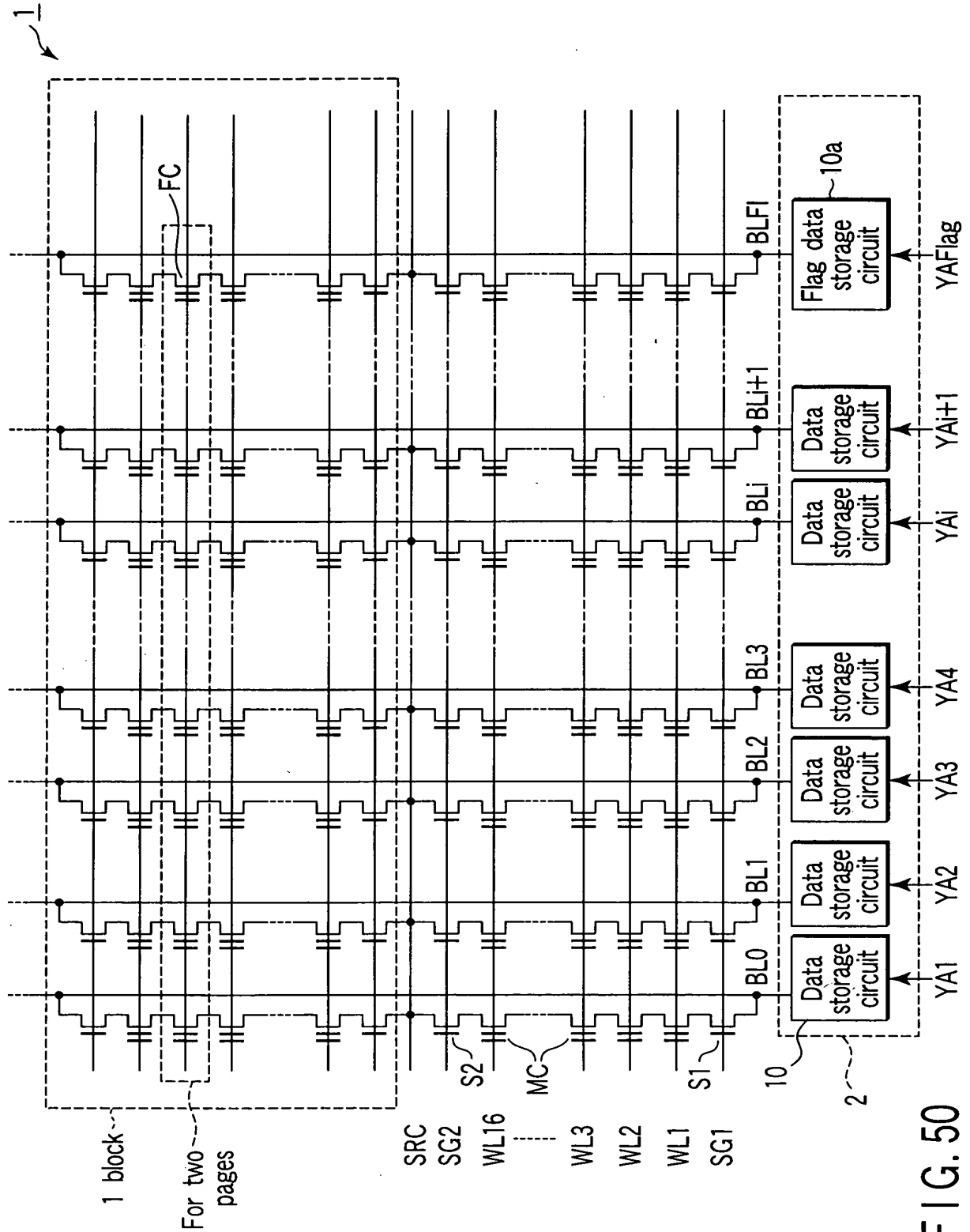


FIG. 50

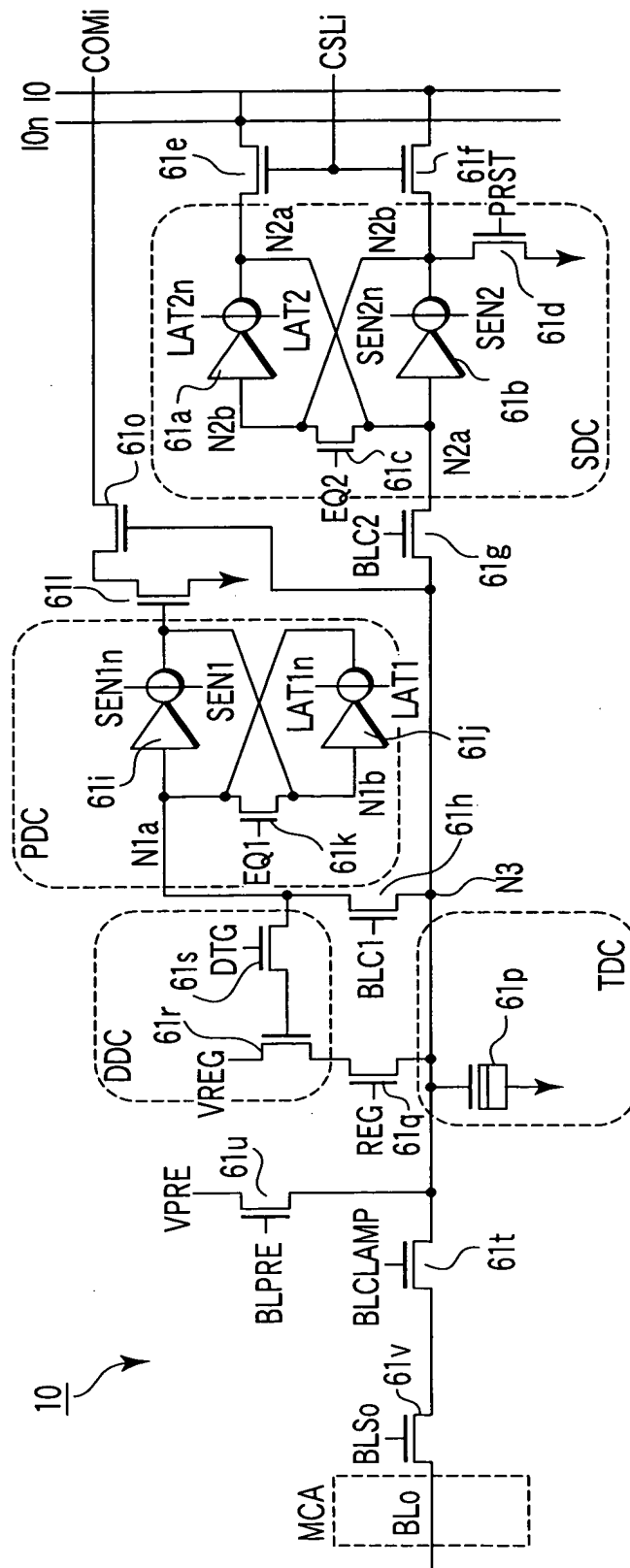


FIG. 51

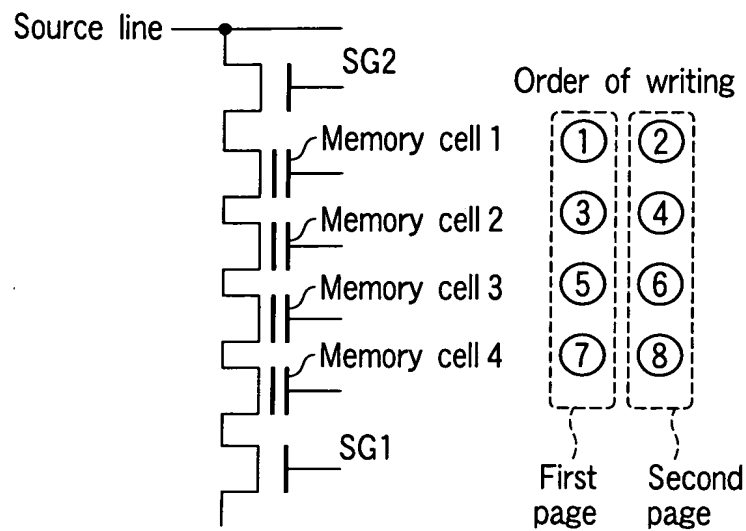


FIG. 52

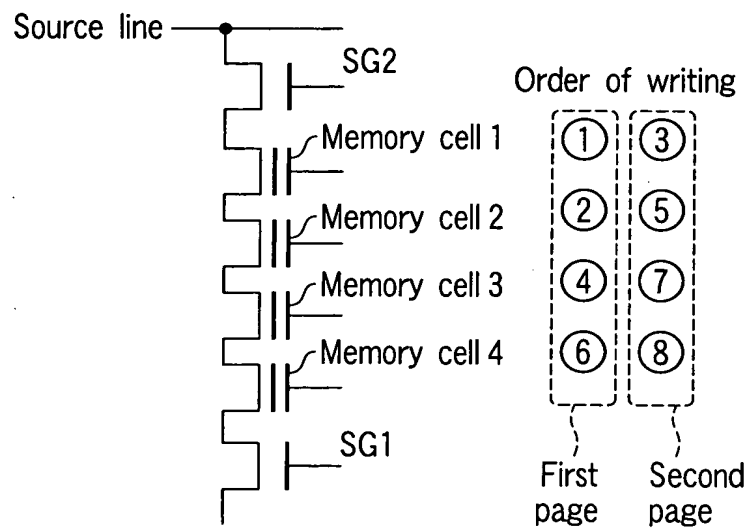


FIG. 53

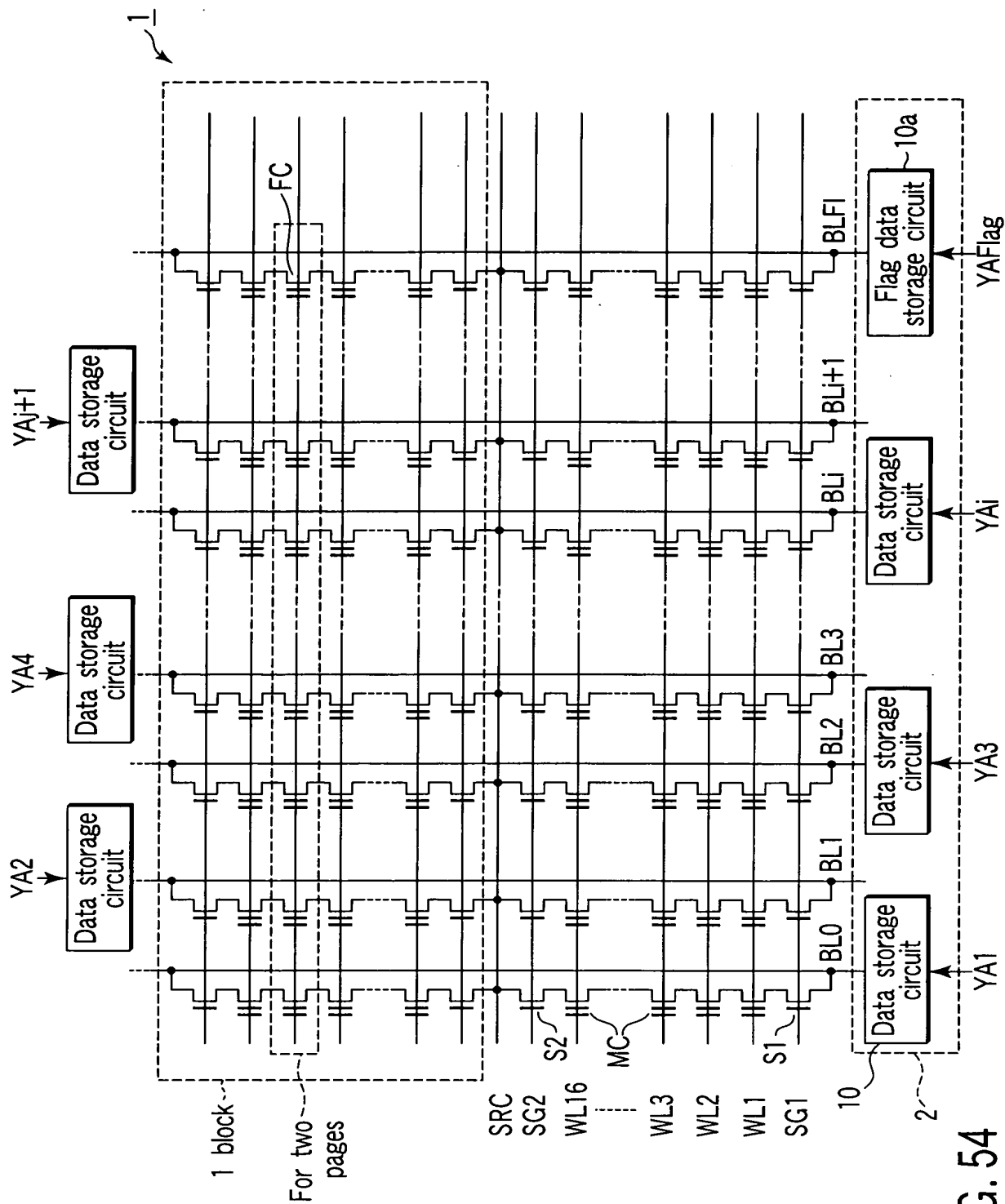
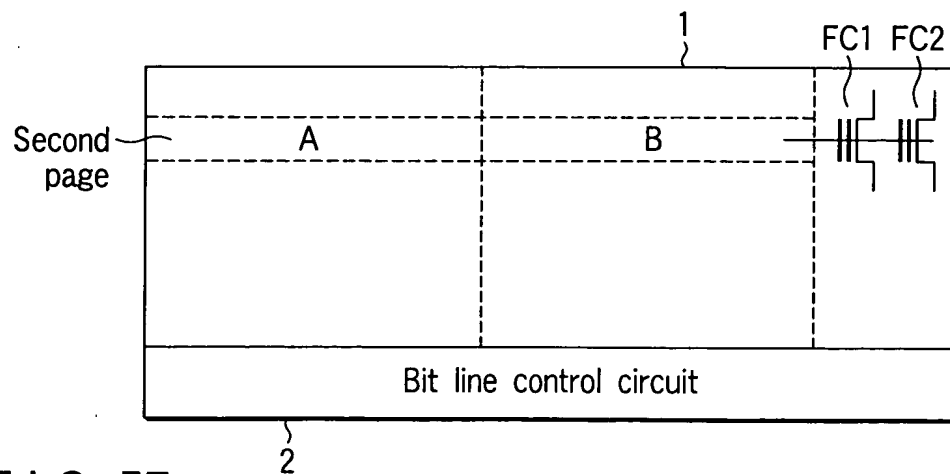
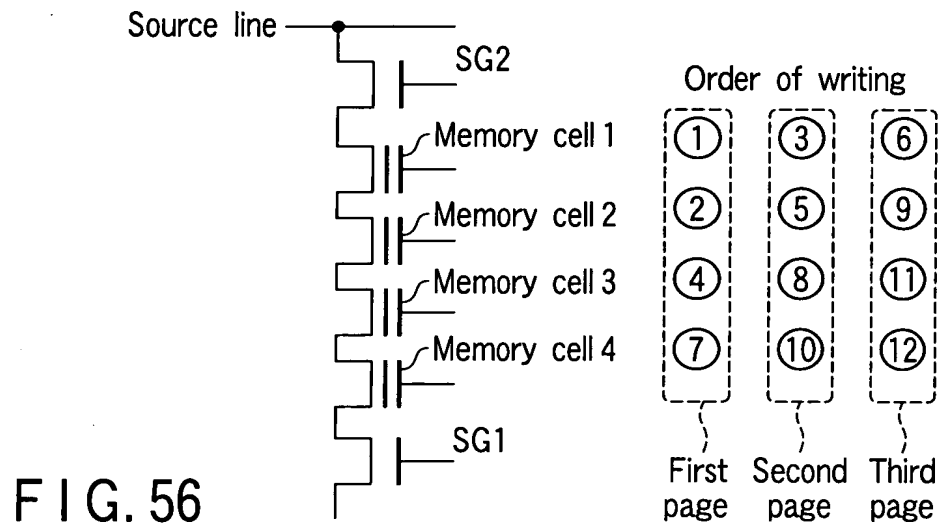
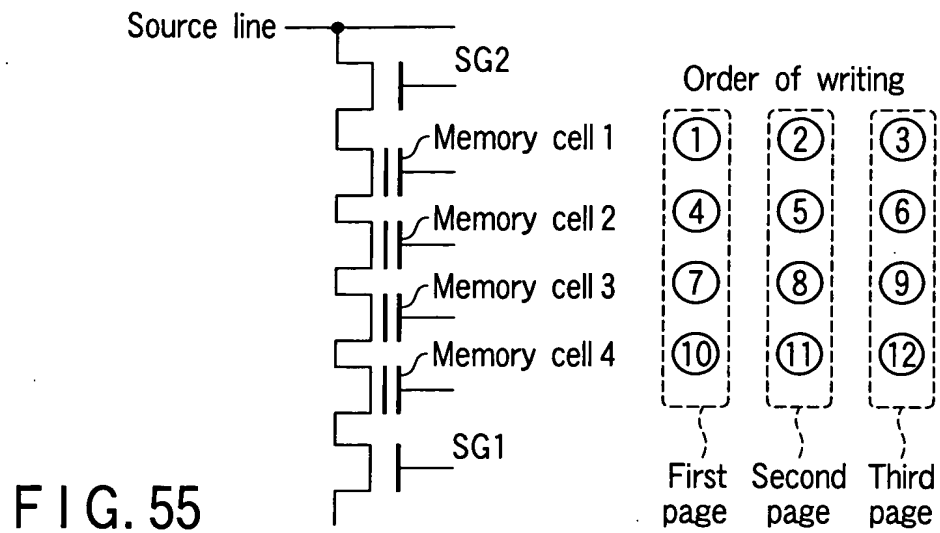


FIG. 54



(Write area A in 1st page)

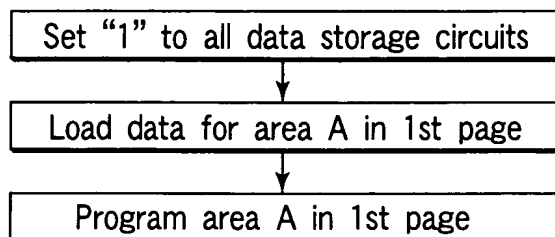


FIG. 58A

(Write area A in 2nd page)

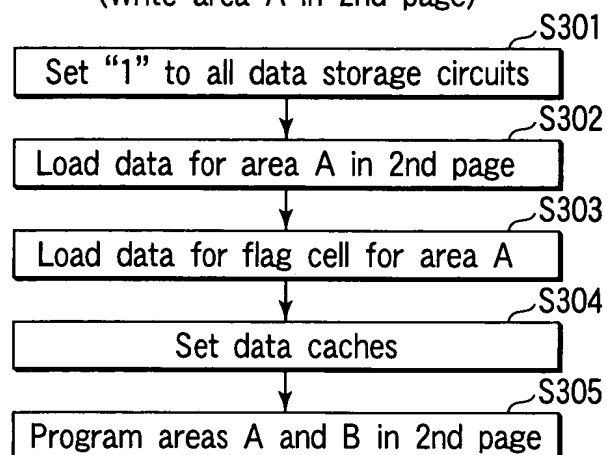


FIG. 58C

(Write area B in 1st page)

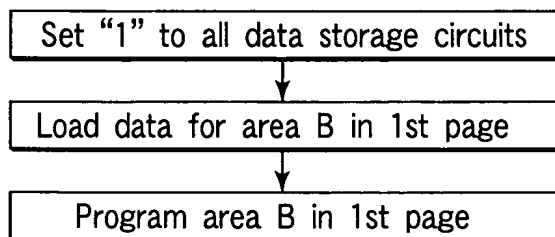


FIG. 58B

(Write area B in 2nd page)

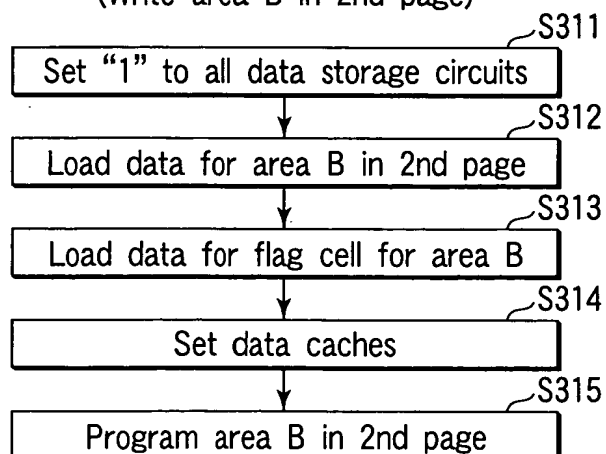
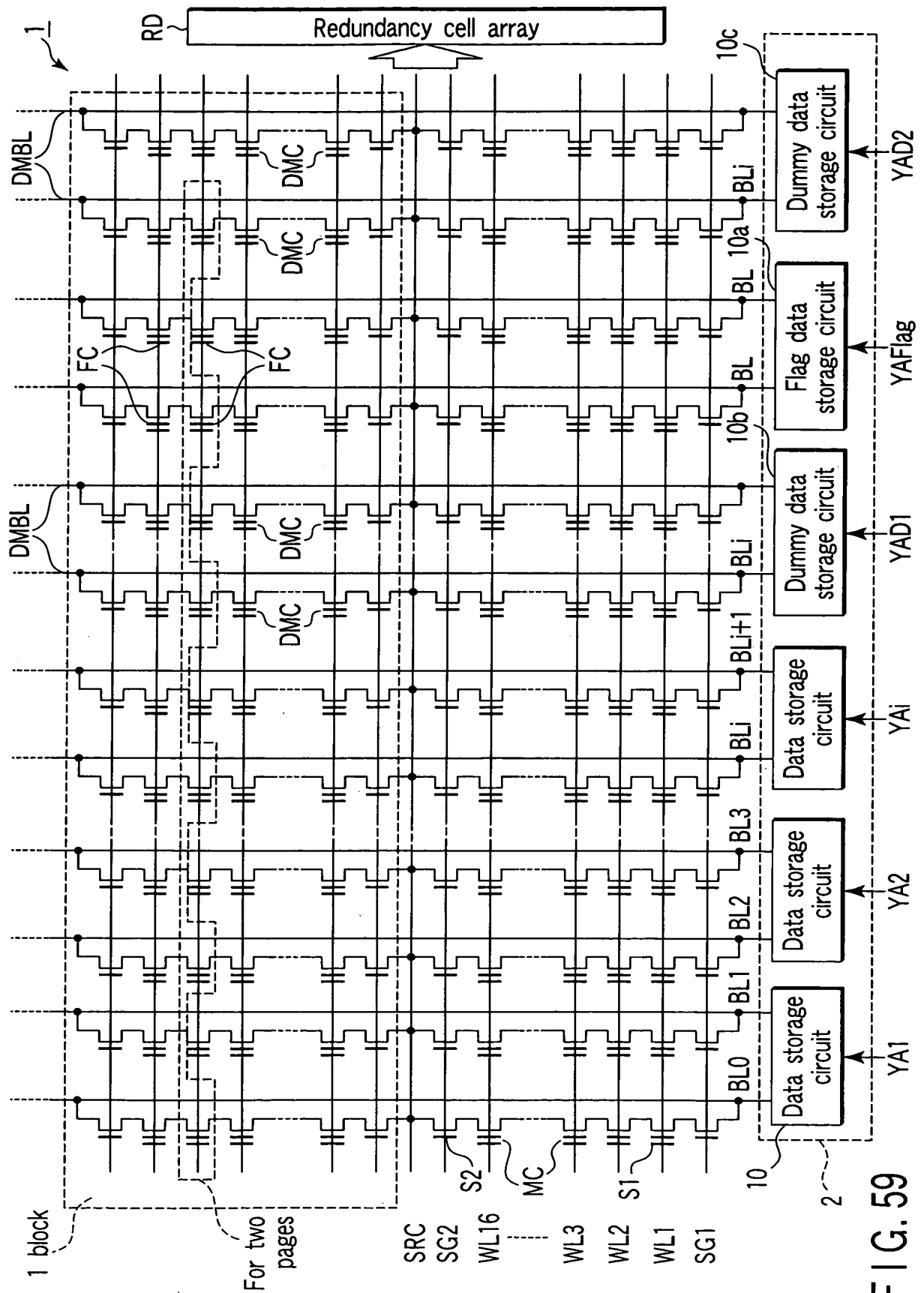


FIG. 58D





After writing the second page

Threshold distribution of a memory cell

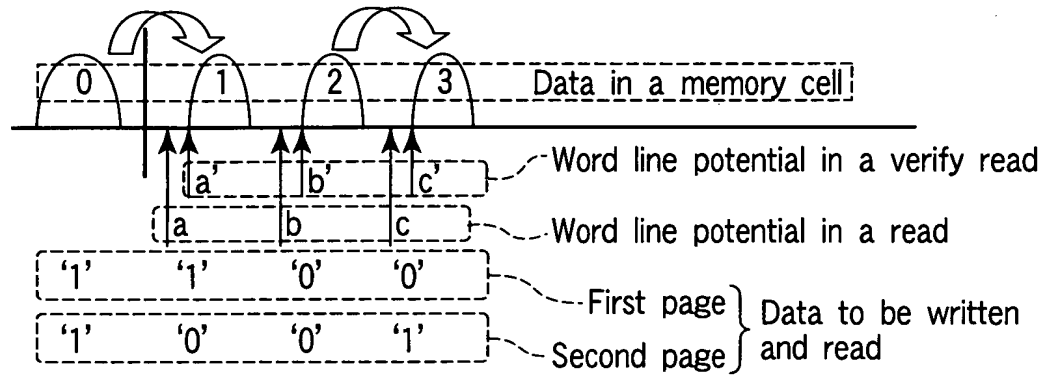


FIG. 60A

After writing the second page

Threshold distribution of a flag cell

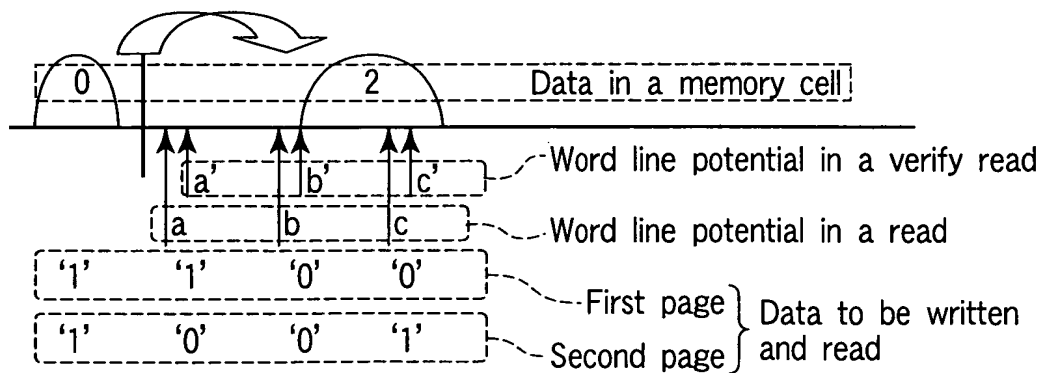


FIG. 60B

After writing the second page

Threshold distribution of the first flag cell

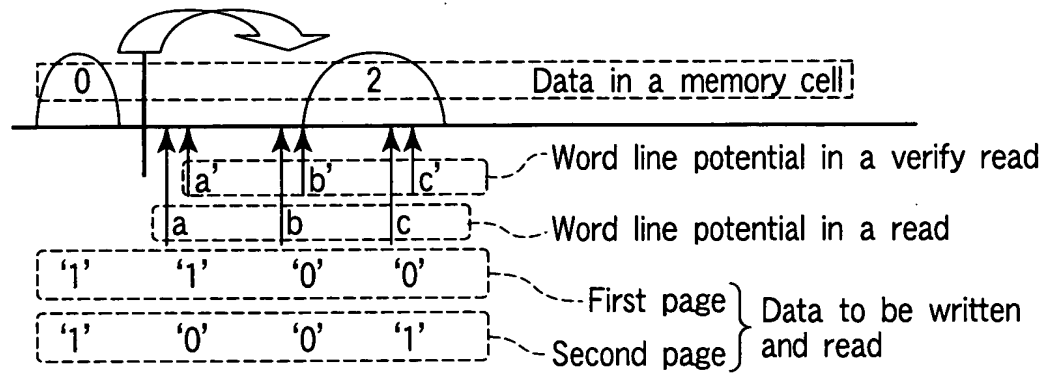


FIG. 61A

After writing the second page

Threshold distribution of the second flag cell

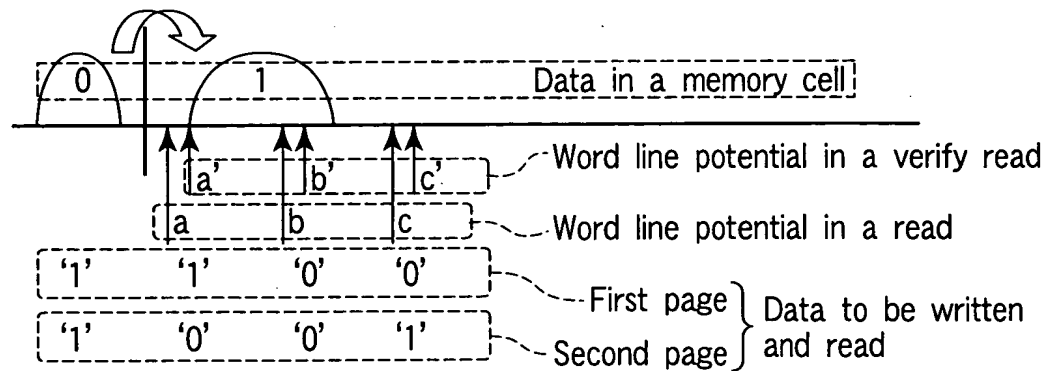


FIG. 61B

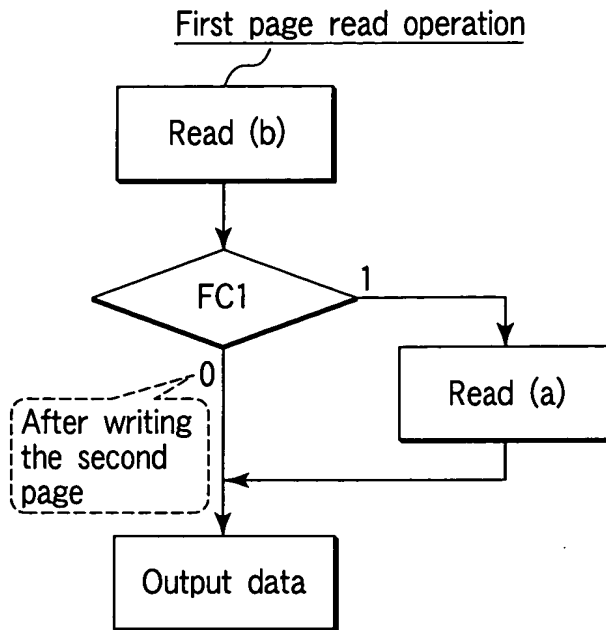


FIG. 62

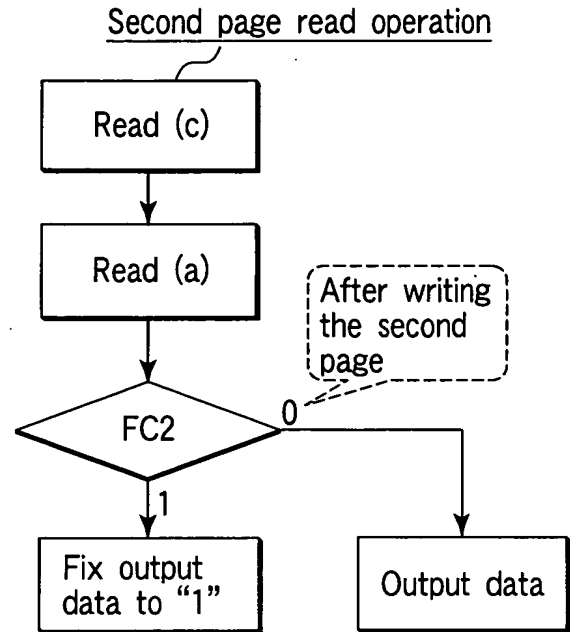


FIG. 63

Memory cell array	BL E	BL 0	BL 0	BL E	BL 0	BL E	BL 0	BL E	BL 0	BL 0	BL E	BL 0	BL E	BL 0	BL E	BL 0
	Dummy cell	Second flag cell	First flag cell	Second flag cell	First flag cell	Second flag cell	First flag cell	Dummy cell	Dummy cell	First flag cell	Second flag cell	First flag cell	Second flag cell	First flag cell	Second flag cell	Dummy cell

FIG. 64